Station Beamforming

SKA-Specifications

	Phase 1	Phase 2
Number of Stations	50	250
Number of antenna per station	11,200	11,200
Core (radius <0.5 km)	50 %	50%
Inner (0,5< radius<2.5 km)	20 %	20%
Mid (2.5< radius<100 km)	30 %	30%
Frequency Range	70 - 450 MHz	70 - 450 MHz
Bits per sample	4	4
Number of beams	480	TBD

Science Specifications

Table 8-2. SKA Phase 1 Technical Requirements Summary

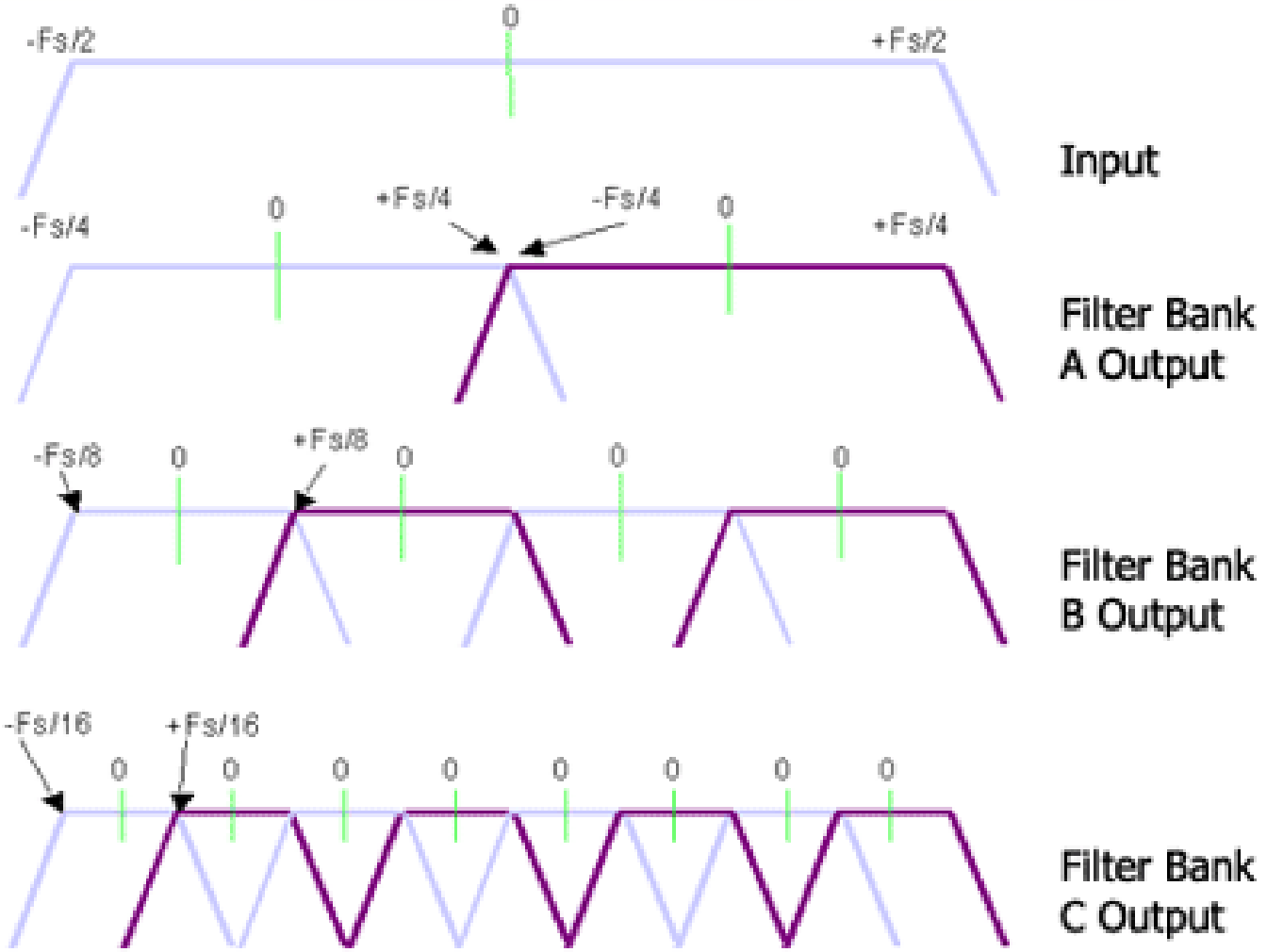
Chapter	Title	Frequency Range (MHz)	Survey Speed (m^4 K^-2 deg^2)	Ae/Tsys (m^2 K^-1)	Frequency Resolution (kHz)	Temporal resolution (s)	polarisation purity	Imaging dynamic range (dB)	Spectral Dynamic Range (dB)	Observation type	Key Science Case Ref	Notes
2	Probing the Neutral Intergalactic Medium during the Epoch of Reionization	70-240	N/A	1000	100	SL	full	N/A	N/A	Line	Probing the Dark Ages	
3	Tracking Galaxy Evolution over Cosmic Time via HI absorption	200-1400	1.0E+07	N/A	5	SL	N/A	35	43	Line	Galaxy Evolution, Large-Scale Structure, & Dark Energy	possible technology change
4	Probing the Epoch of Reionization with the 21-cm Forest	70-240	N/A	N/A	0.2	SL	N/A	N/A	61	Line	Probing the Dark Ages	
5	Pulsar Surveys with the SKA1	400-3000	N/A	1000	10	5.00E-05	N/A	N/C	N/C	Time Domain	Strong Field Tests of Gravity Using Pulsars and Black Holes	non-imaging data required
6	Pulsar Timing with the SKA1	800-3000	N/A	10000			40 dB	N/C	N/C	Time Domain	Strong Field Tests of Gravity Using Pulsars and Black Holes	high frequency agility required, non imaging data required, polarization purity likely needs to be achieved only on-axis, post-calibration
7	Additional Telescope Considerations	70-10,000					full-field capability	74 dB capable			multiple	"forward capatibility"

Station Processing Remit

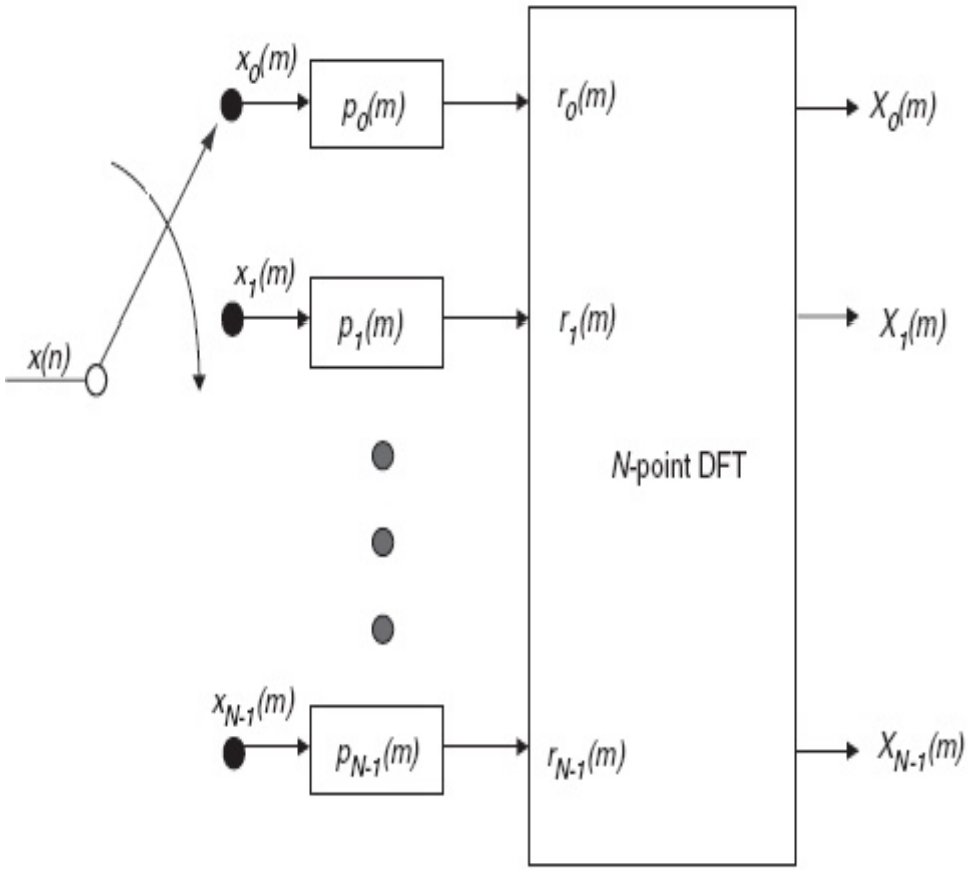
- Temporal-filtering (Channelisation)
- Spatial-filtering (Beamforming)
- Calibration of RF-chain
- Band-pass correction
- Early RFI-mitigation
- Bit-count limitation
- Produce correlator-ready inputs

Channelisation

Channelisation

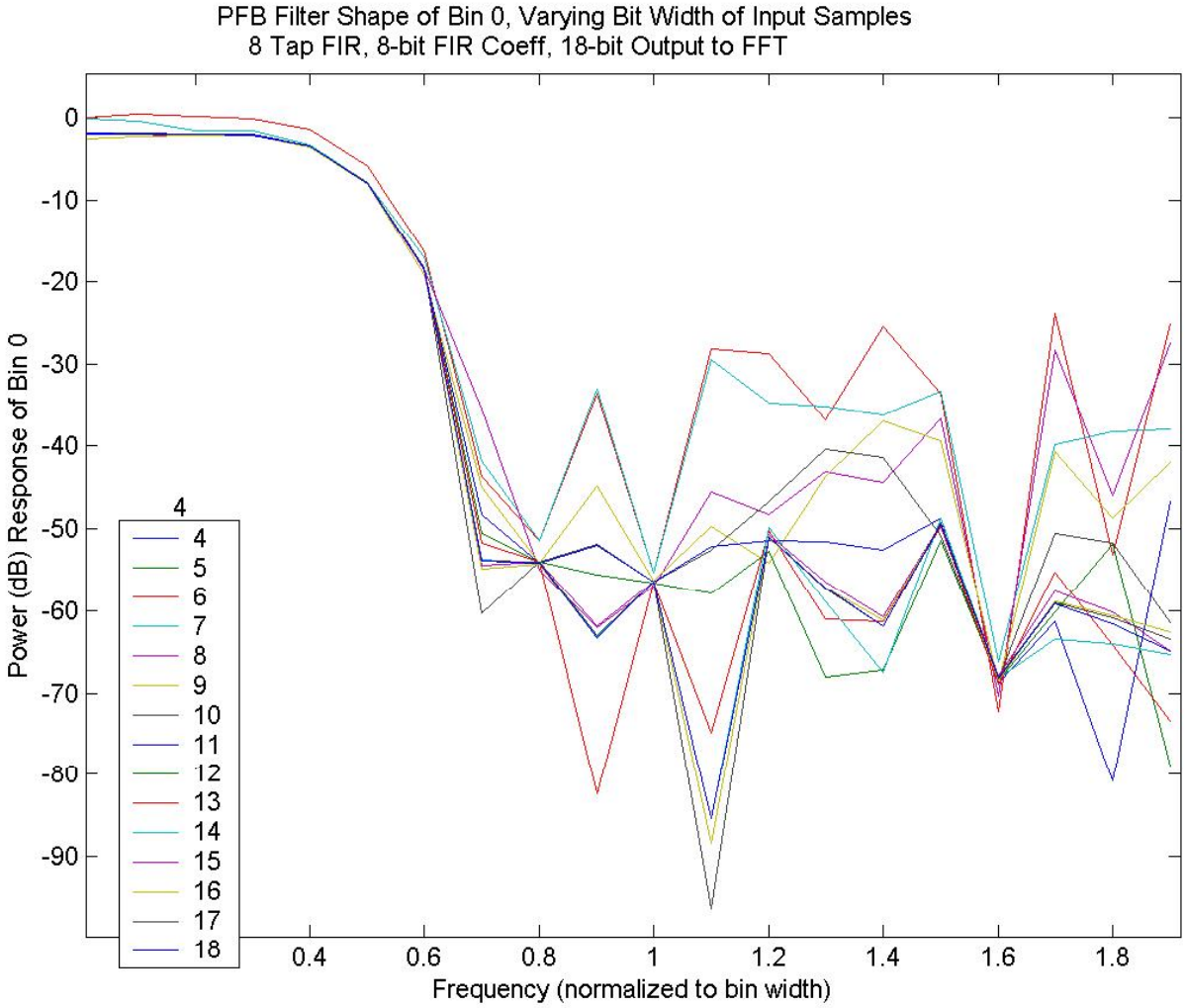


Polyphase filterbank

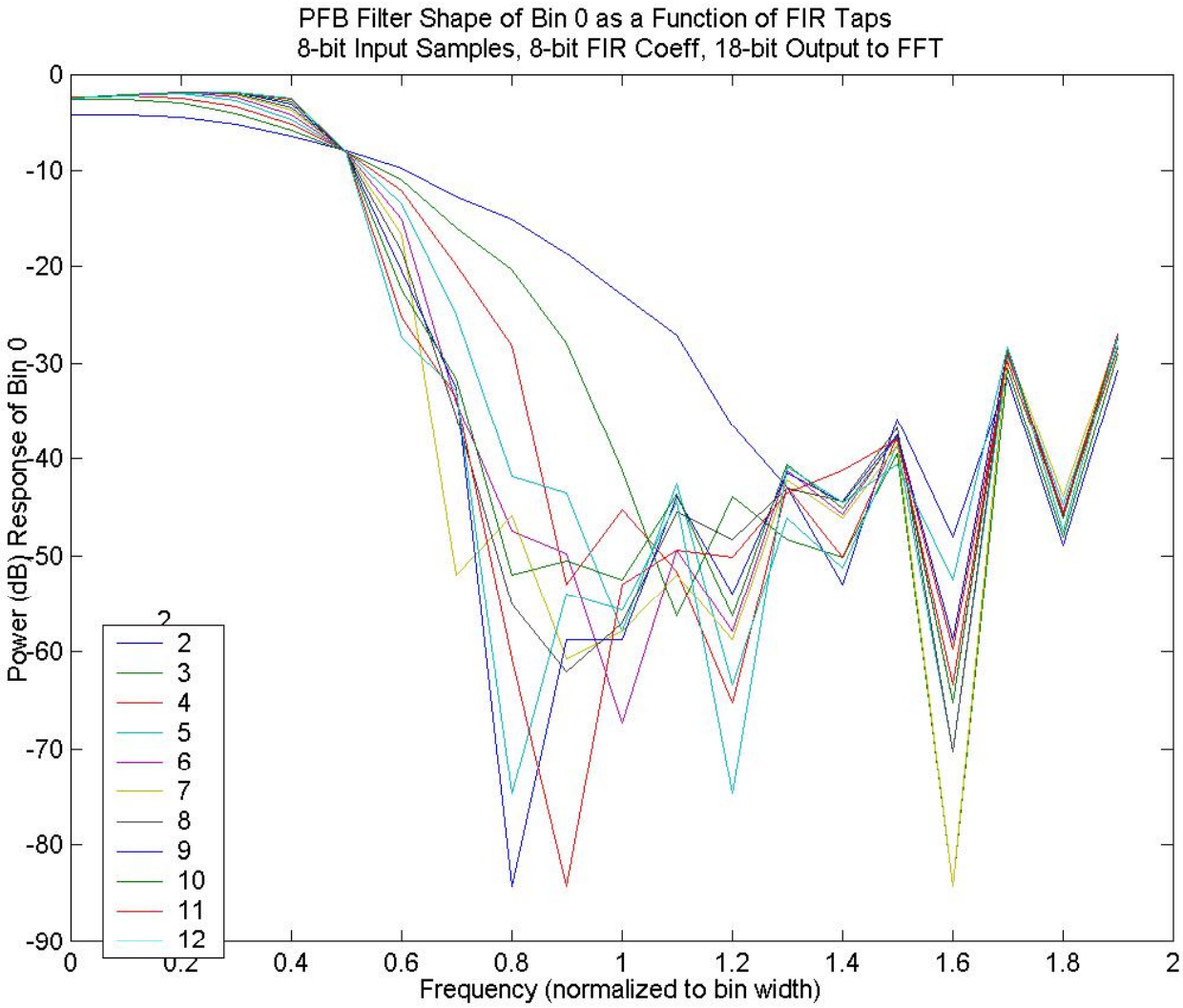


- Scales as N_{chans} log N_{chans}
- ≈16TOP/s for 65536 channels i.e. ≈ 6kHz channels
- Can either be done per element or per beam
- Best to do it hierarchically interleaving beamforming with channelisation
- But can be done on a single-chip (CMOS-65nm ≈ 1W)

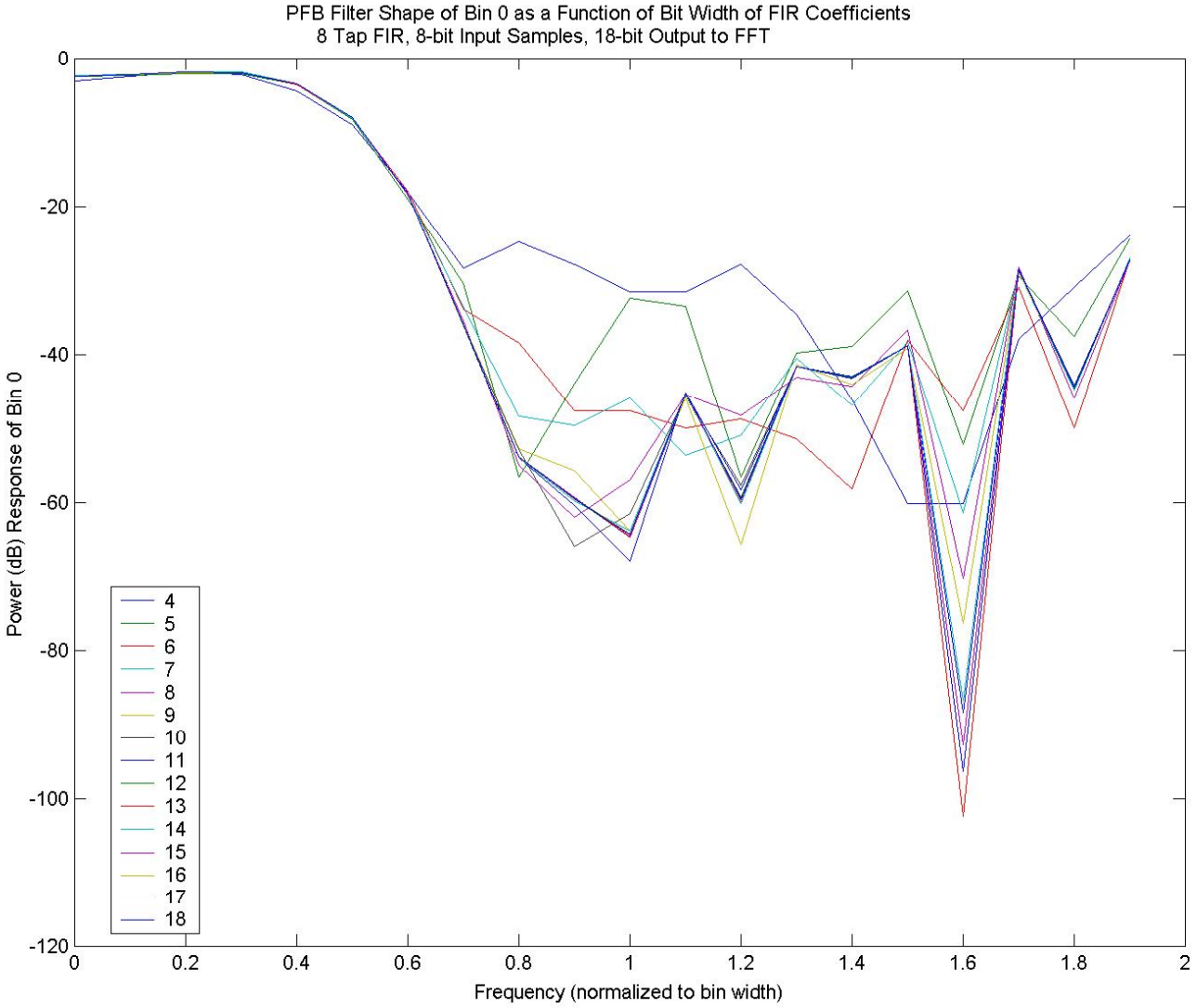
Filter Characteristics



Filter Characteristics

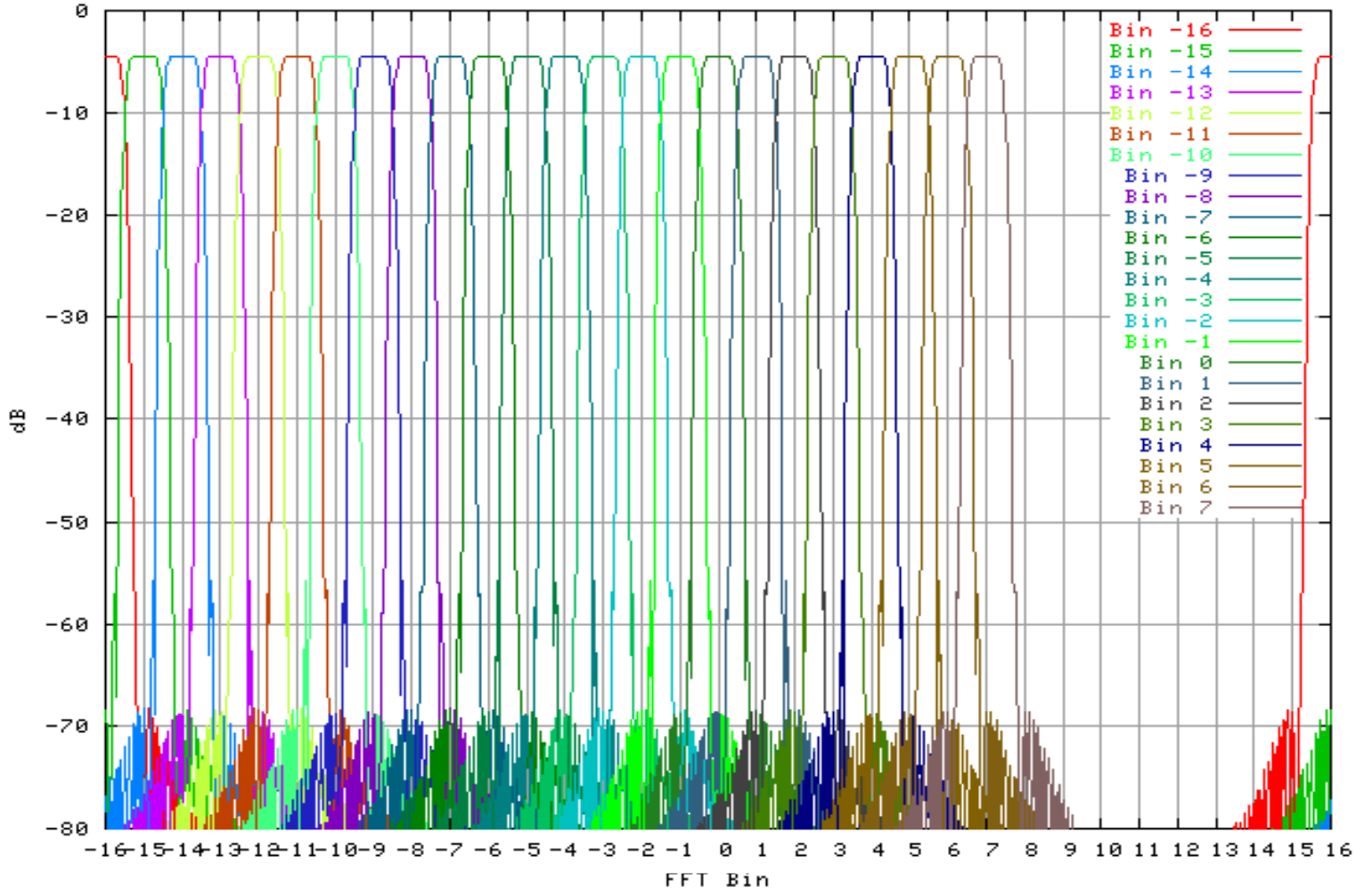


Filter Characteristics



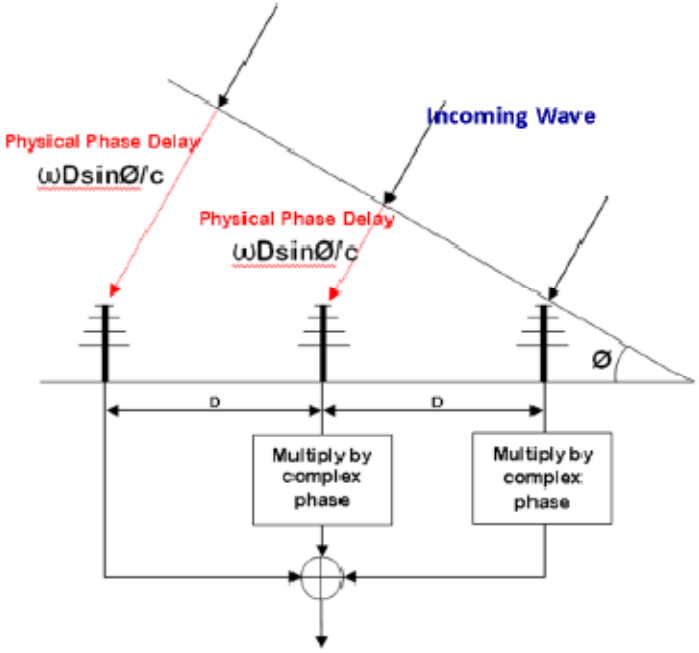
gest radio telescope

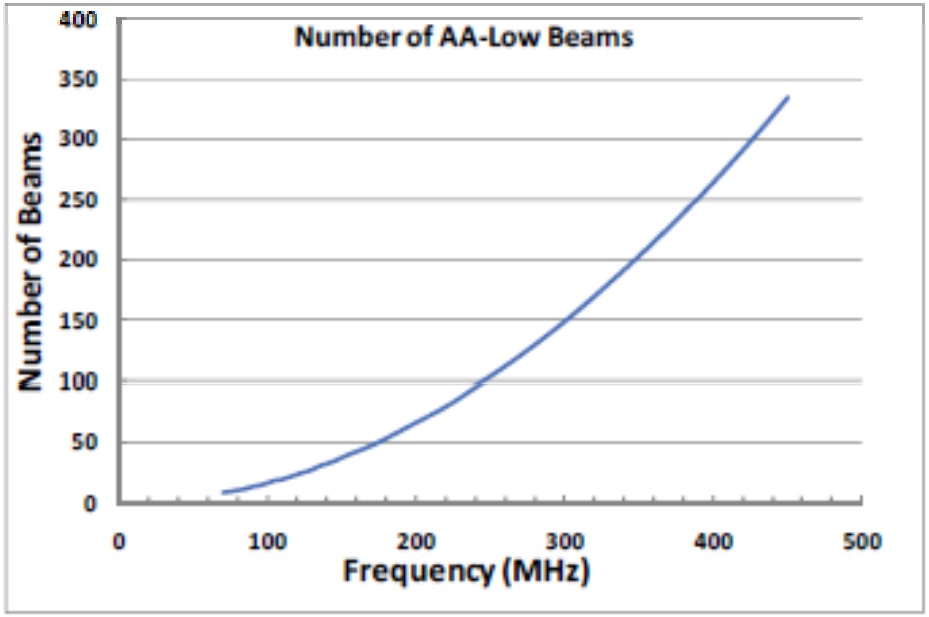
Filter Characteristics



Beamforming

Beamforming

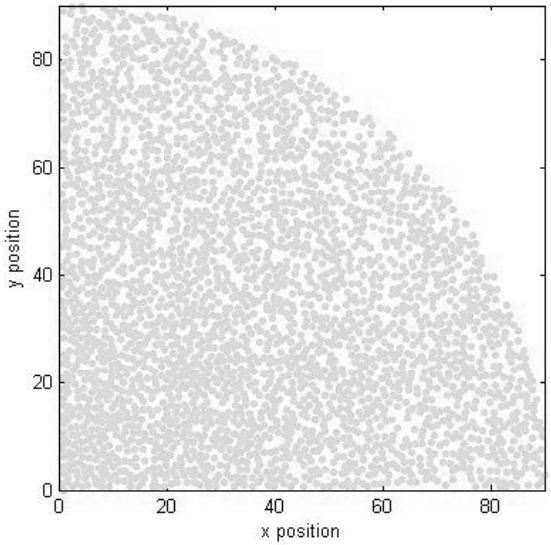


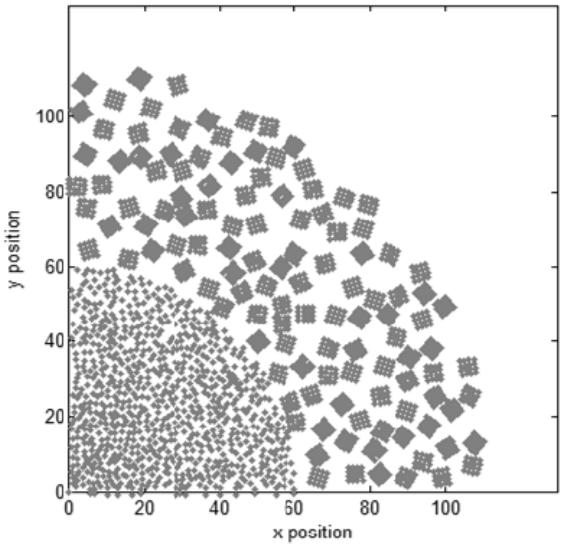


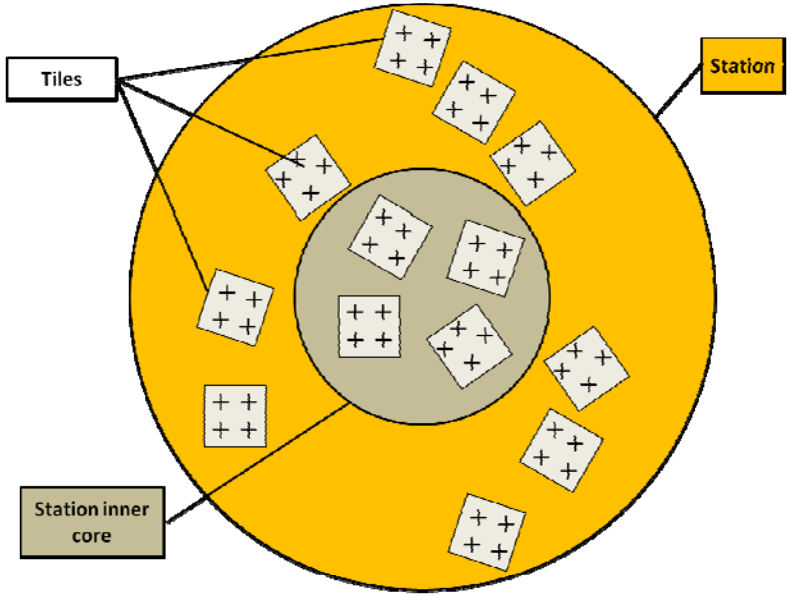
Beamforming

- Possible options:
  - Time-domain beamforming
  - Phase-Shift beamforming
- Possible technology options:
  - RF-beamforming
  - Digital beamforming
- Possible Layout options:
  - Either single-stage beamforming requiring: $N_{elements} \times N_{beams} \times N_{channels}$
  - Hierarchical beamforming requiring different amount of beams per tile
- Calibration options vary depending on scheme, but a station correlator will be required to calibrate the signal paths and delays to ensure correct beamforming

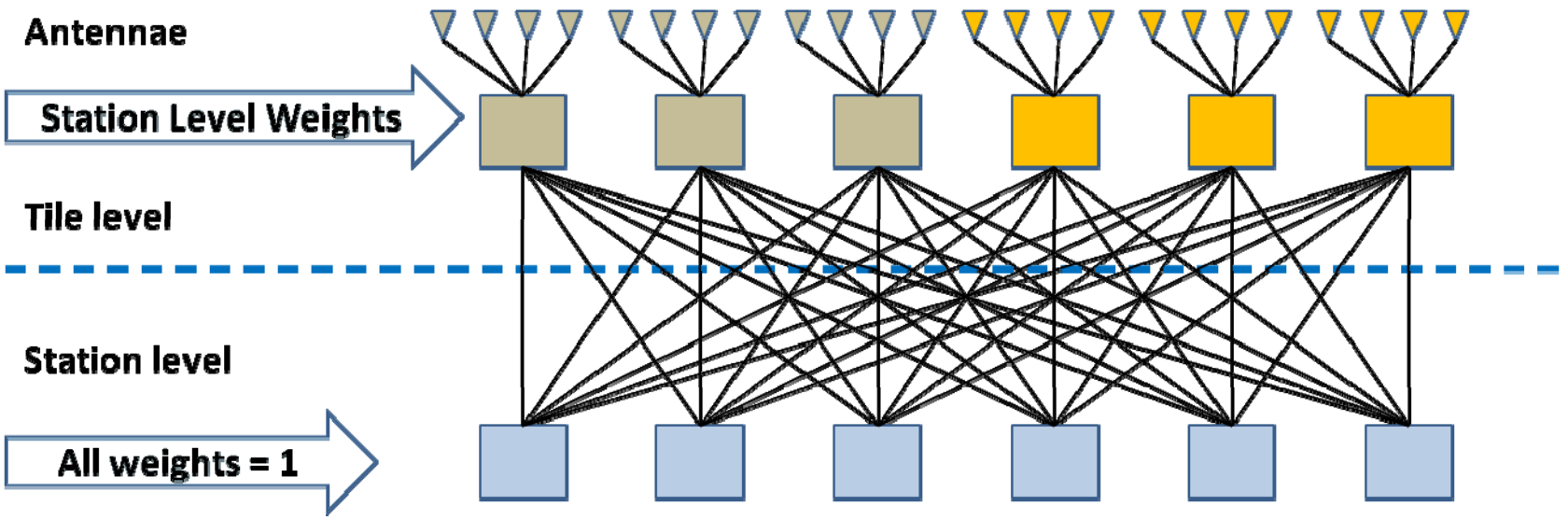
Station Layout



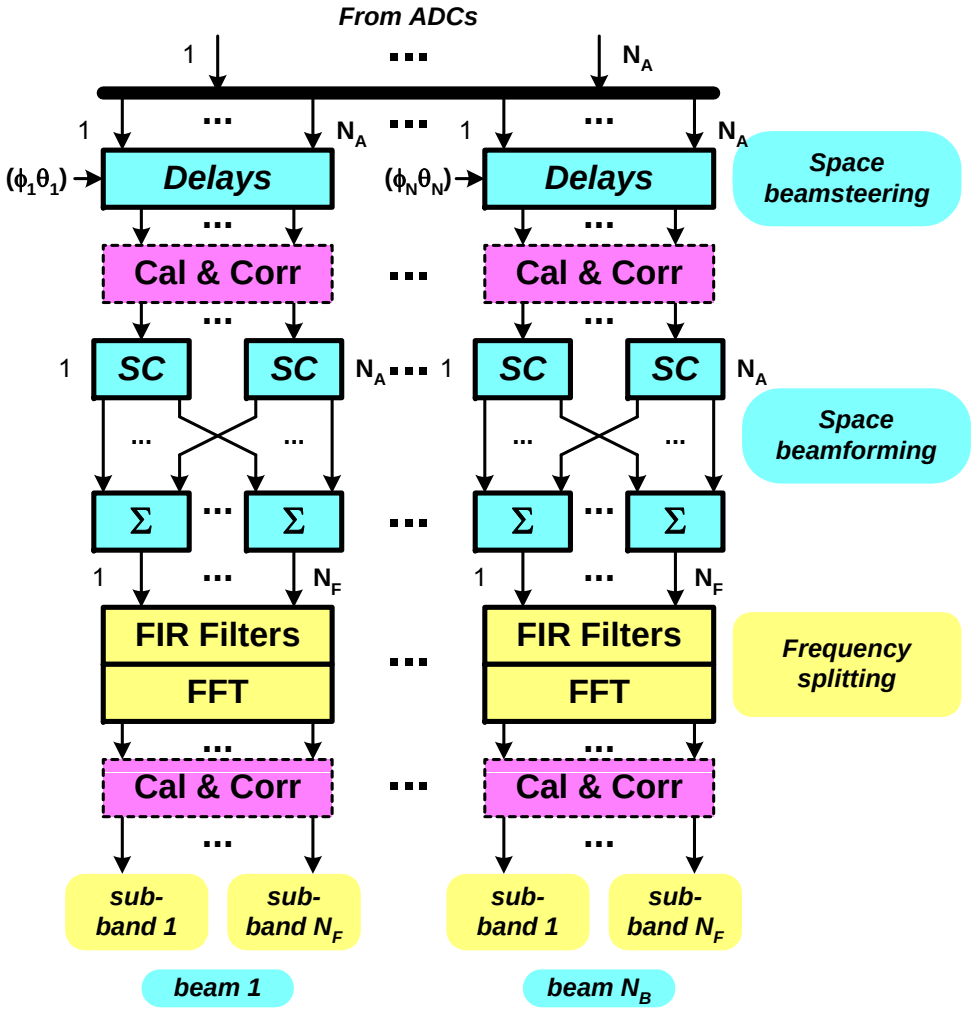


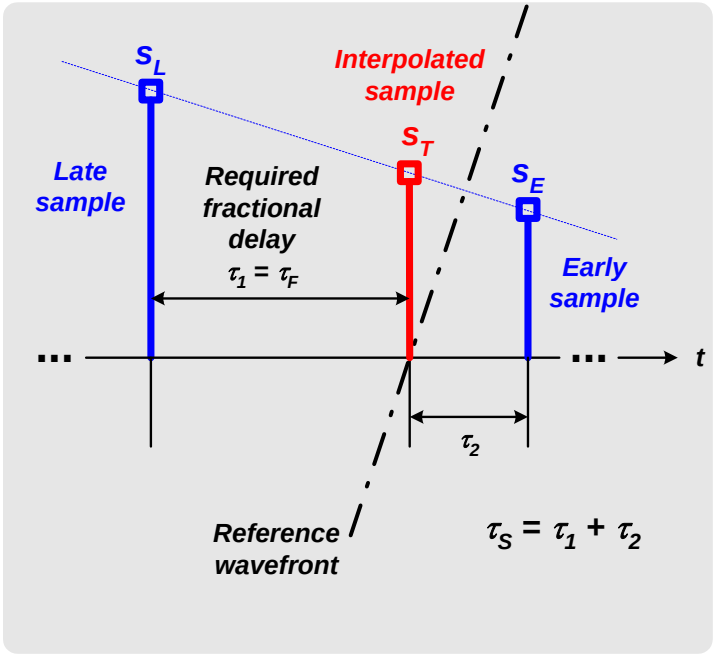


Hierarchical Beamforming



Space-Frequency Beamformer





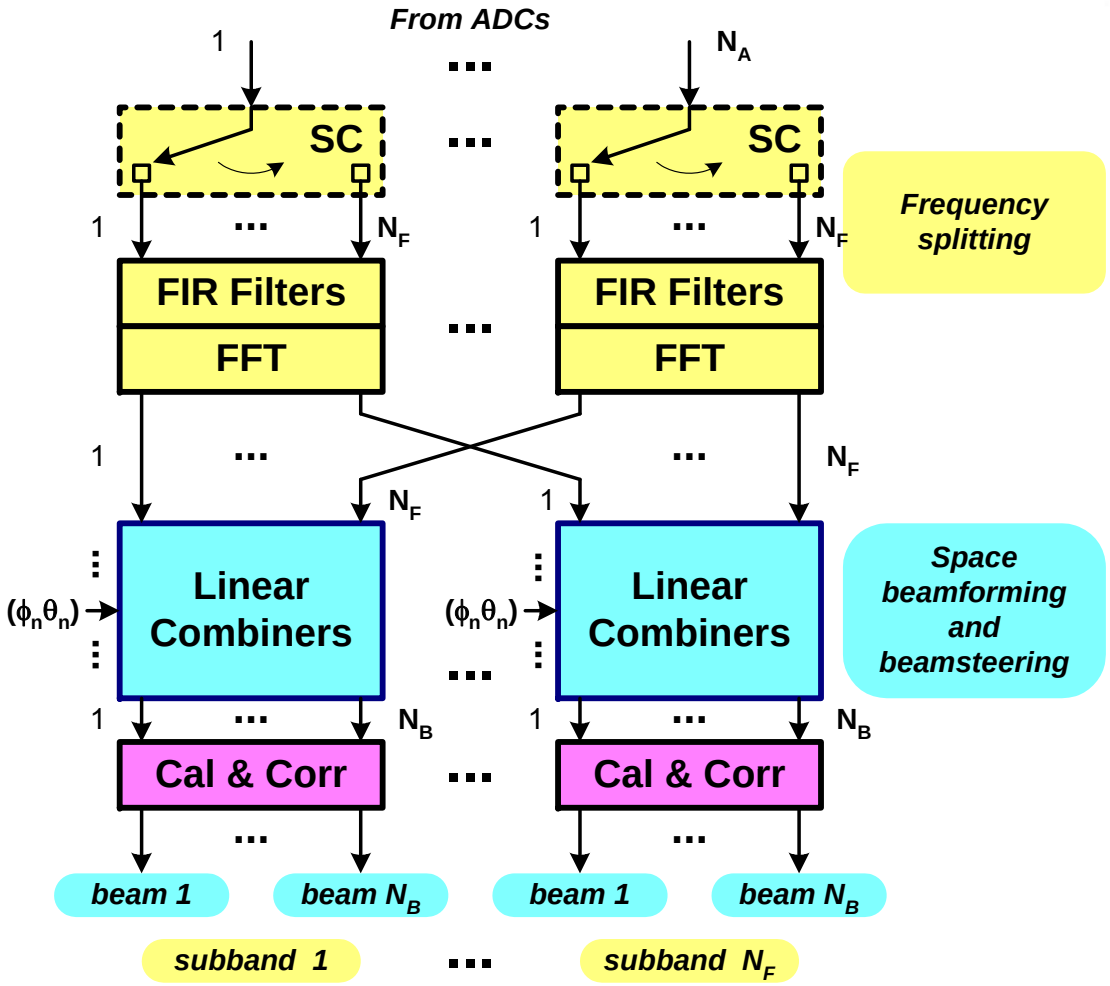
Time-domain beamforming

- *Silicon gate based keyed delay banks*,
- *FIR-filtering/up-sampling* based, HW-level realizations consisted of FIFO structures for integer (coarse-grained) delaying and FIR filters for fractional (fine-grained) delaying,
- *Linear interpolation/up-sampling*, SW-level implementations that imply re-indexing of data samples for integer delaying and time-domain linear interpolation of successive samples for fractional delaying,

Space-Frequency BF

- $M_{SF1} = O\{N_A N_B\}$
- At the second “frequency” stage of processing, the FS-beamformer should perform about
- $M_{SF2} = O\{2N_B N_F \log_2 N_F\}$
- real multiplications. The total number of operations is
- $M_{SF} = M_{SF1} + M_{SF2} = O\{N_B(N_A + 2N_F \log_2 N_F)\}$

Frequency-Space beamformer



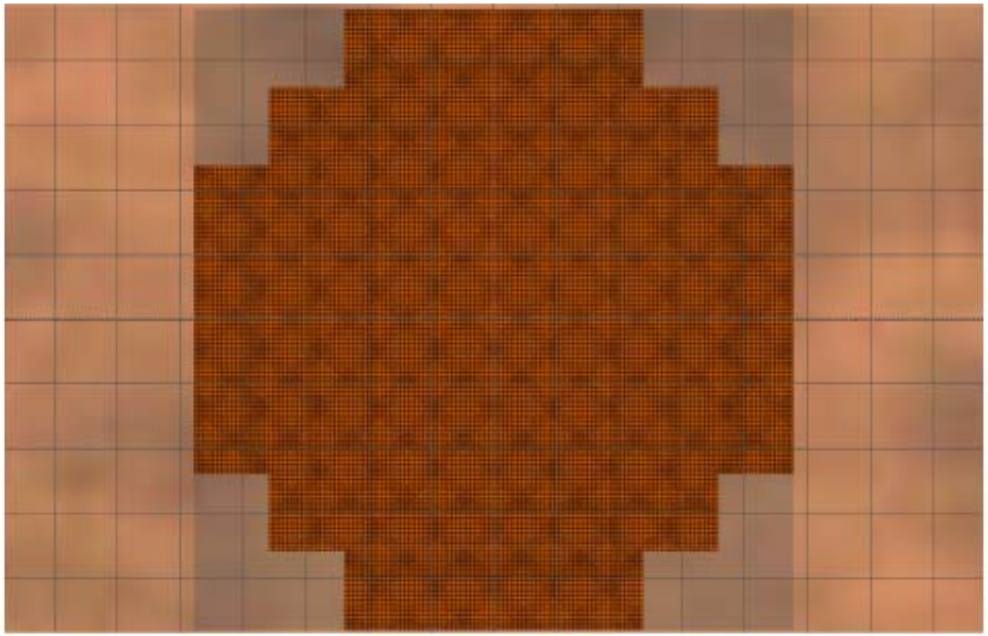
FS-Beamforming

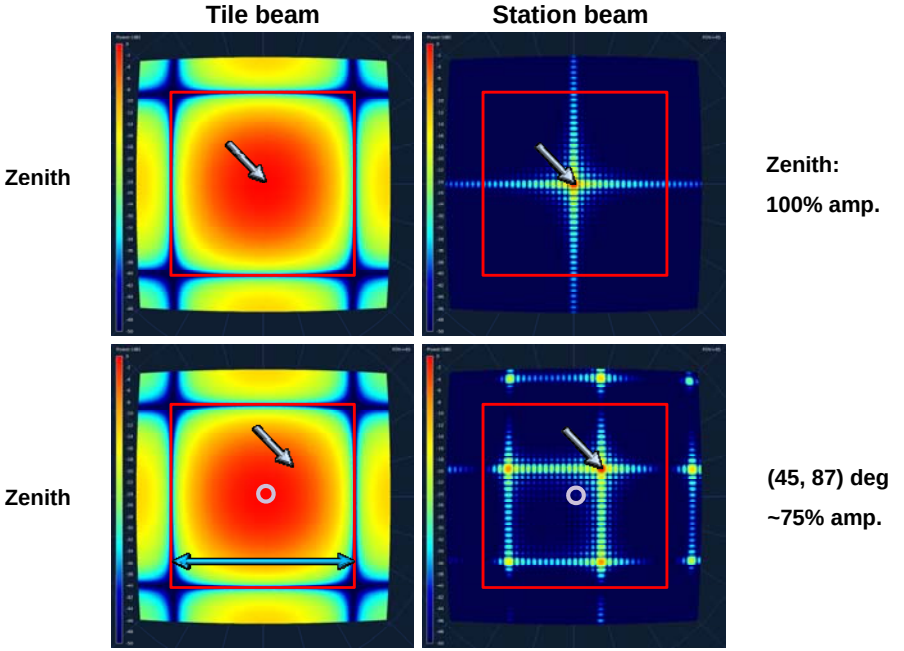
- $M_{FS1} = O\{2N_A N_F \log_2 N_F\}$
- $M_{FS2} = O\{4N_B N_A N_F\}$
- $M_{FS} = M_{FS1} + M_{FS2} = O\{2N_A N_F(\log_2 N_F + 2N_B)\}$
- For SKA-1: SF-Beamforming is cheaper by a factor of 1000

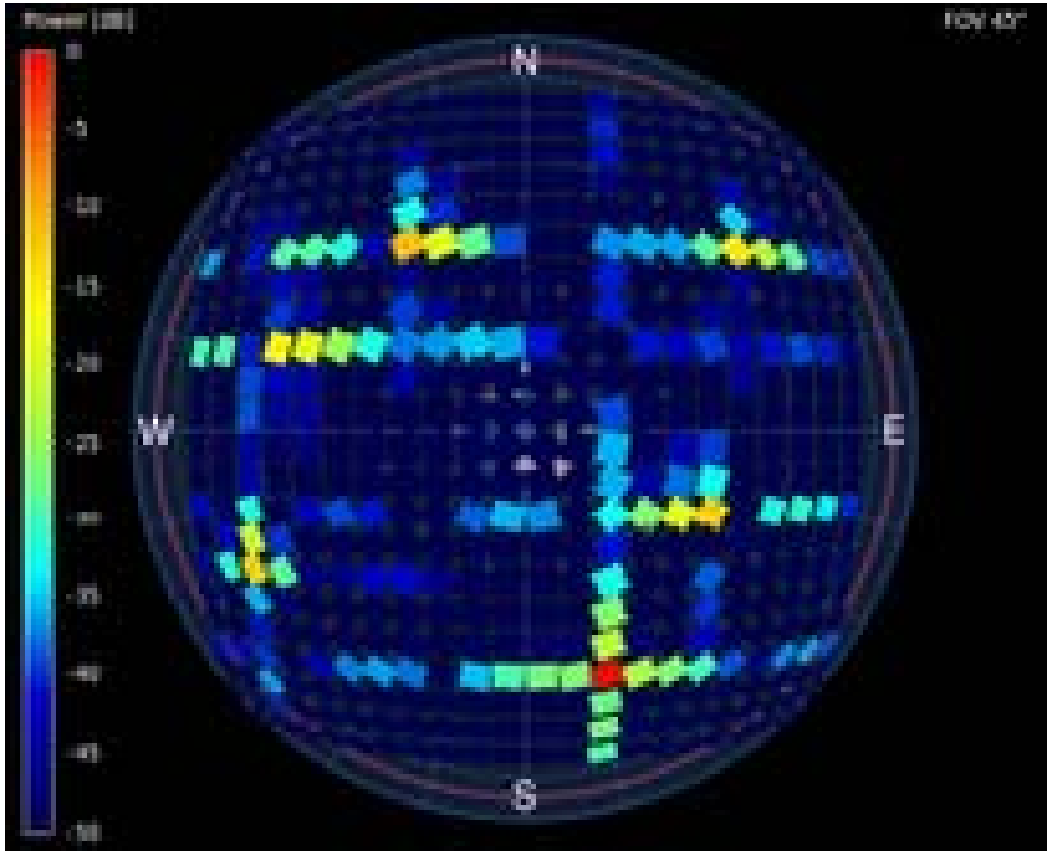
Beamforming Scheme Comparison

Beamforming Scheme	Operation Count
Single Level DFT	16 TOP/s
Gridding + FFT	5.2 TOP/s
Hierarchical 2-level + DFT	320 GOP/s

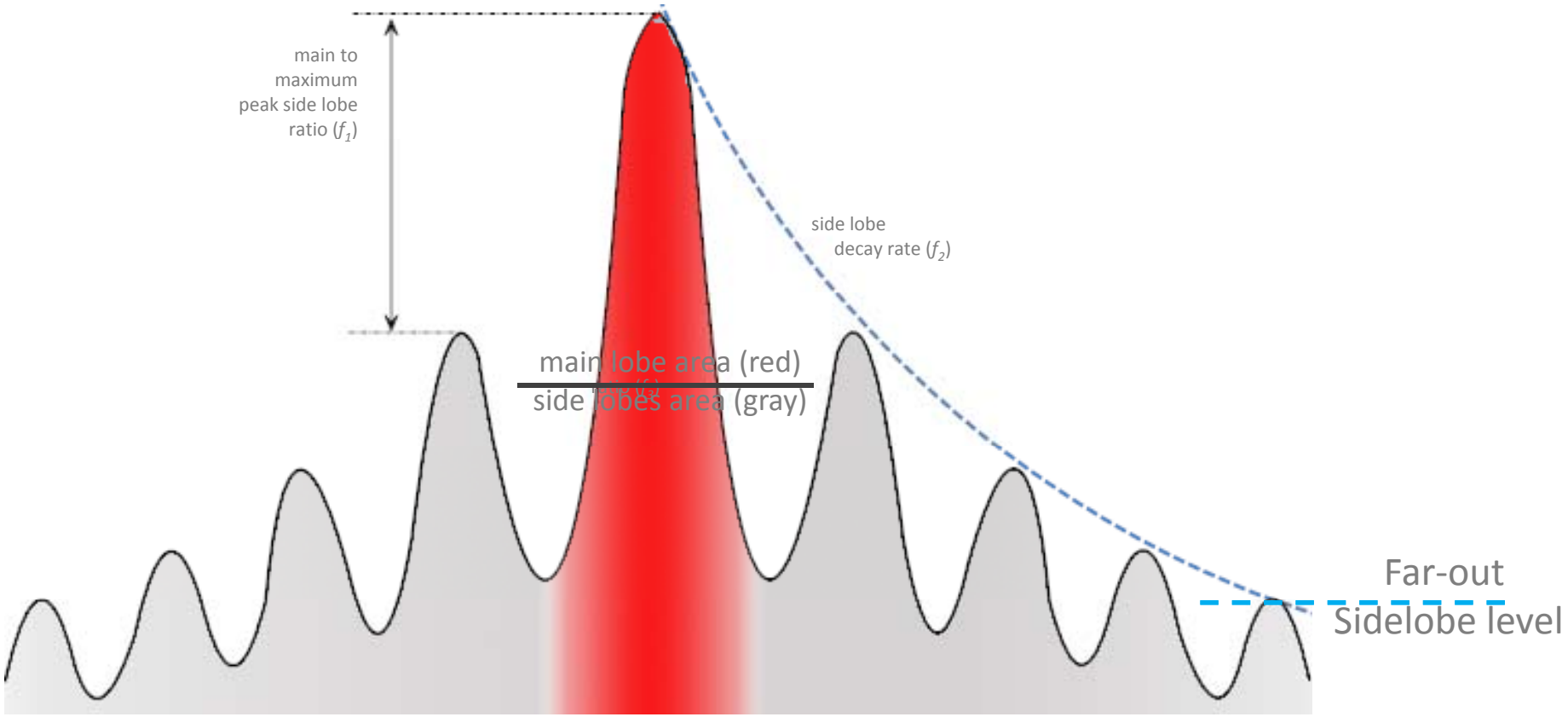
Simulations





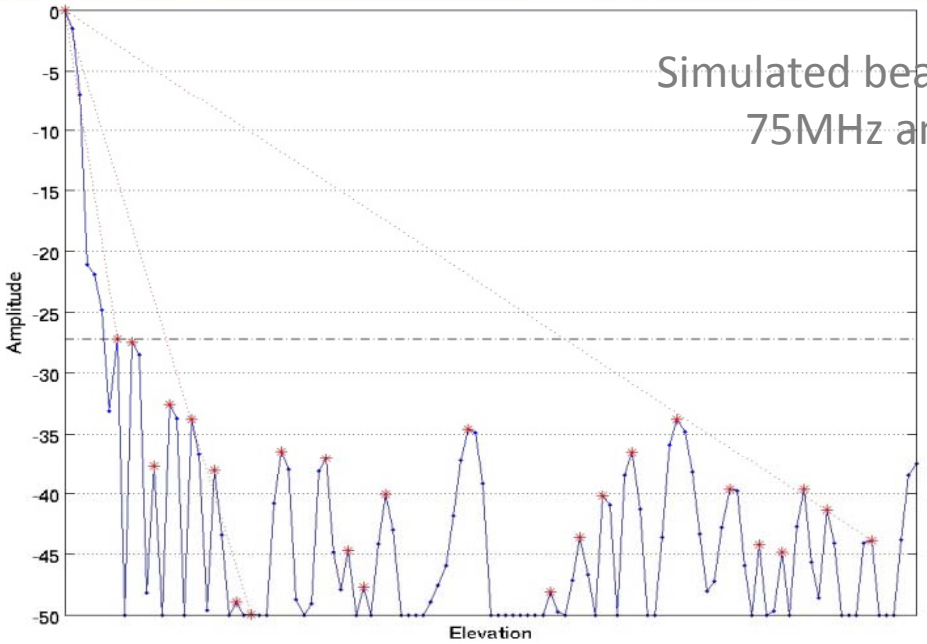

N
W
E
S

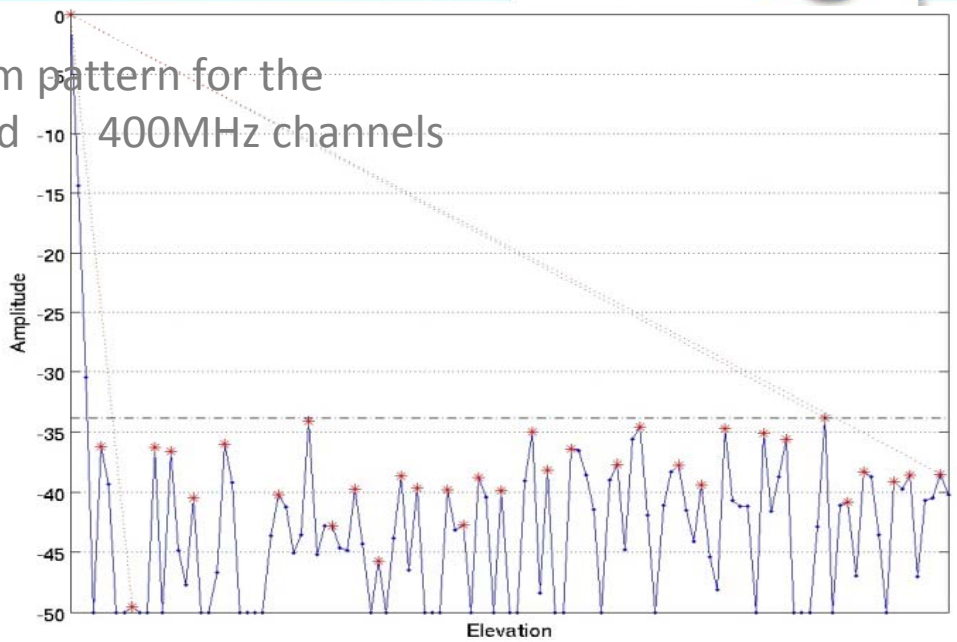
Dynamic Range



Simulations

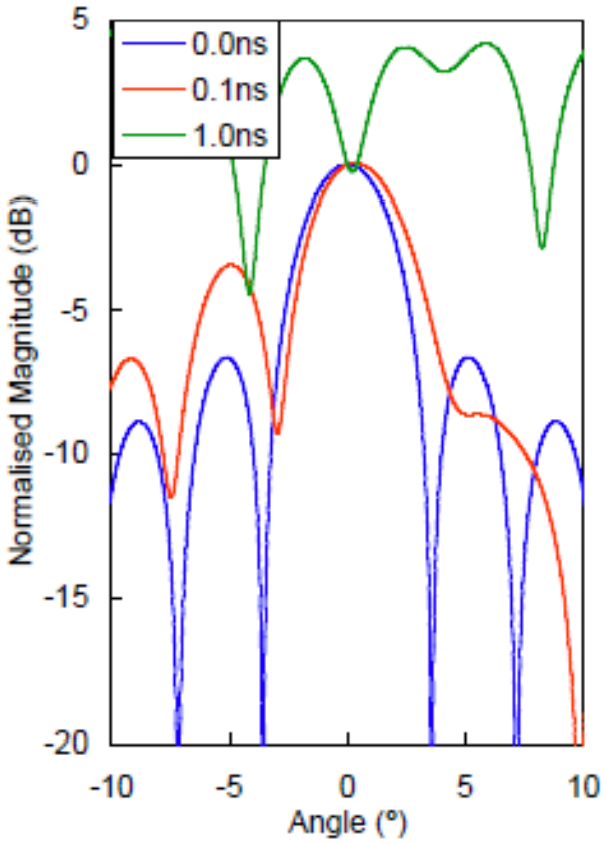
Simulated beam pattern for the 75MHz and 400MHz channels

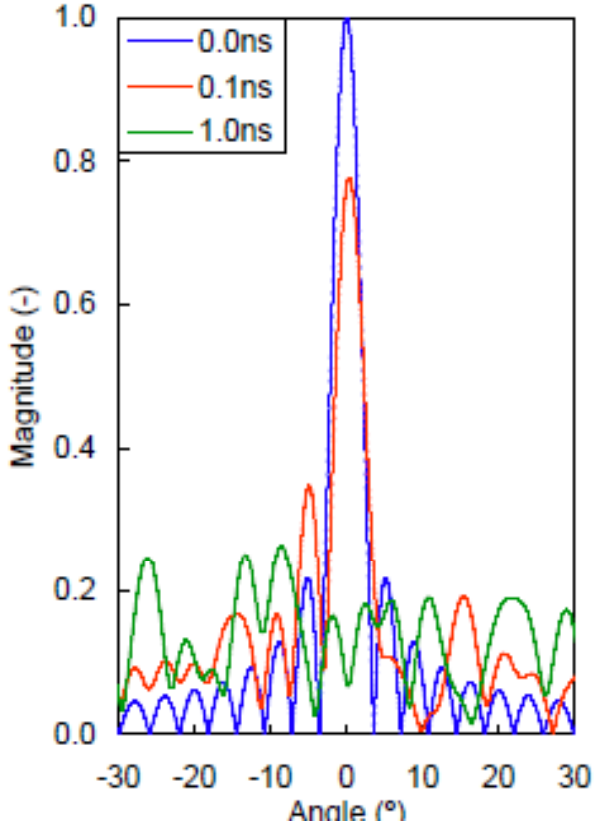




	First side lobe (dB)	Min side lobe (dB)	Max side lobe (dB)	Average side lobe level (dB)	Fitness 1	Fitness 2	Fitness 3	Final fitness
Channel 1	-27.1714	-49.9606	-27.1714	-38.1618	0.4566	0.3456	N/A	0.8021
Channel 2	-26.7919	-48.2191	-26.6408	-37.6890	0.4672	0.4023	N/A	0.8695
Channel 3	-49.5531	-49.5531	-31.3922	-37.5158	0.3722	0.0288	N/A	0.4010
Channel 4	-37.7337	-44.8757	-31.3988	-36.6110	0.3720	0.1378	N/A	0.5098
Channel 5	-36.2520	-49.5274	-33.8700	-37.3937	0.3226	0.0451	N/A	0.3677

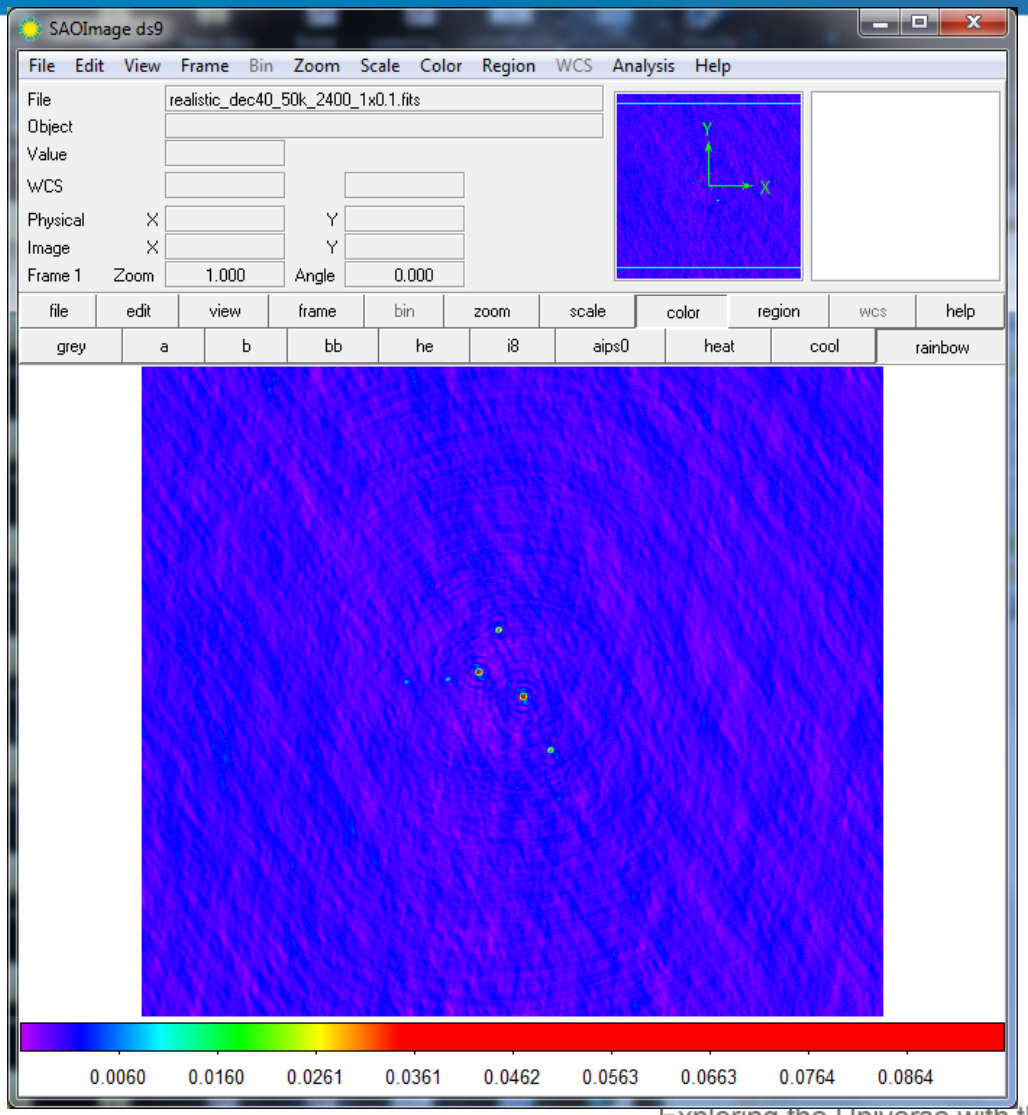
Phase and Amplitude Calibration



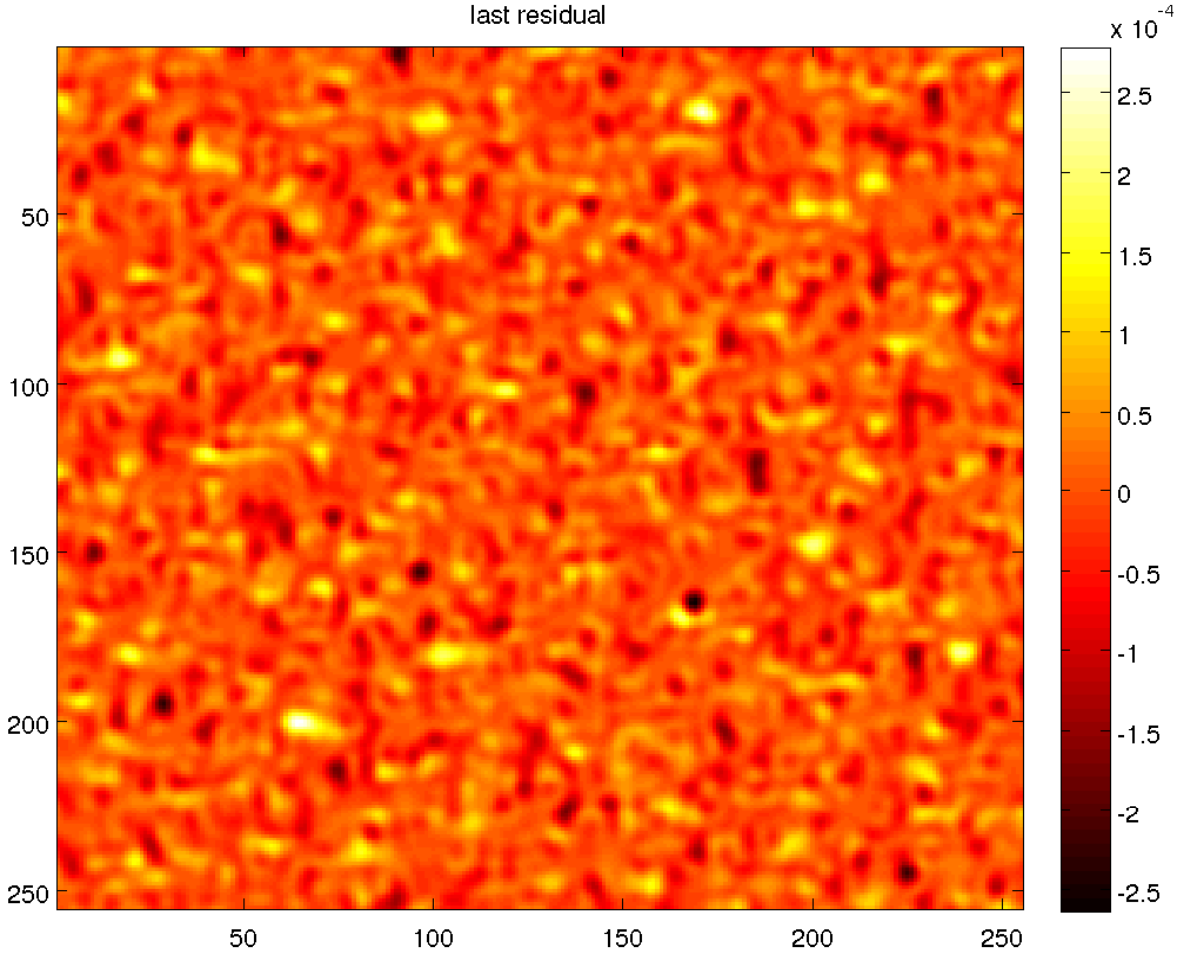


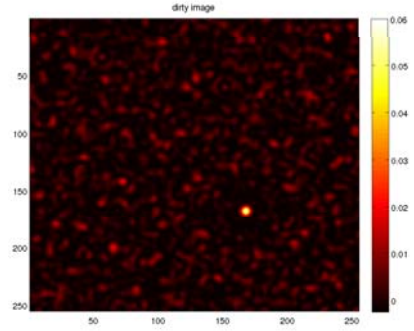
This is why calibration of the RF-chain is imperative and each station will require a correlator

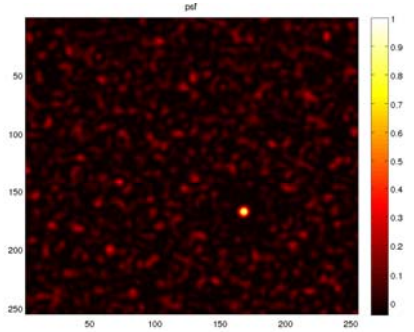
Imaging Dynamic Range



- Station configuration: c3_random_antennas_25x11200
- Number of rotations: 120
- Rotation time increment: 1s



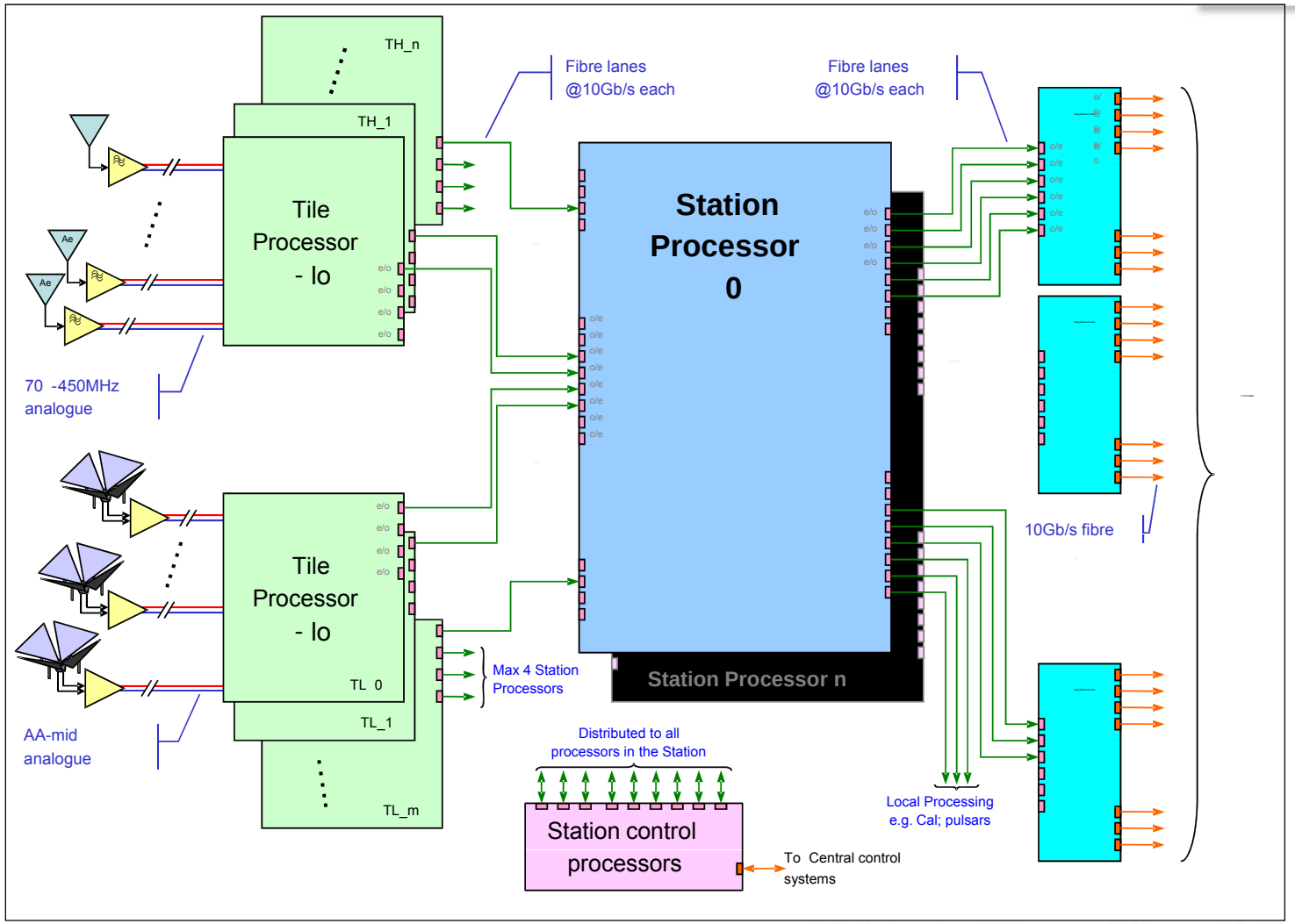




he world's largest radio telescope

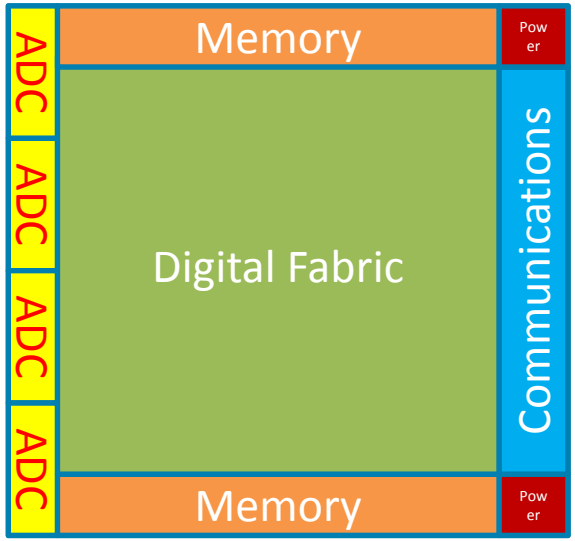
Path to Implementation

Schematic Diagram



Station Processing ASIC

8 of these chips are placed on a tile Processing board to handle:
64-dual polarised antennas



Each ASIC has:
128Gb/s input B/W and
1 TOP/s and
≈ 1Mbit of memory
And 32Gb/s output B/W

ASIC Specifications

Parameter	Values	Units
Clock Rate	250	MHz
Power Consumption	10	W
Performance	1	TOP/s
Input Bandwidth	128	GBit/s
Number of Beams	4	X2 polarisations
Number of Channels	256	
Polyphase filter-length	8	Taps
Polyphase filter-coefficients	16	Bits
Beamforming co-efficients	12+12	Bits
Output Bitwidth	4+4	Bits
Memory Capacity	1	MBit
Communications Capability	Yes	
Calibration capability	Yes	
Control capability	Yes	

Cost and Power Estimates

Description	Qty	Cost ea	Power ea	Total Cost (excl. NRE)	Total Power
Front-End ASIC in tile processor	3000	$10	80W	$30,000	240kW
Tile Processing board	200	$1000	20W (additional to ASIC)	$200,000	15kW
Station Processing Board (including backplane)	200	$1000	100W	$200,000	20kW
CX4-Cables	1000	$10	0W	$10,000	
Station Processing Rack	10	$1000		$10,000	100kW
Infrastructure/Cooling	1	$100,000		$100,000	100kW
Totals:				**≈0.5M**	≈500kW

Resource Allocation

Tile-Processor Chip Design + test	2 man years + 1 man year	$5M
Tile-processor board design + test	2 man years + 1 man year	$0.5M
Station Processor Chip design + test	2 man years + 1 man year	$2M
Station processor board design + test	2 man years + 1 man year	$2M (depending on FPGA/ASIC architecture)
Station processor firmware design + test	2 man years + 1 man year	$0.5M
Mechanical rack design	1 man year	$0.25M

Risk Register

Risk	Effect/Mitigation
Proposed beamforming and channelization scheme does **NOT** meet specifications.	The required dynamic range and sensitivity is not reached. This can be mitigated by prior simulation and/or another scheme developed.
Processing architectures consuming too much power.	Operating costs and reliability of the processing chains are affected. This can be mitigated by de-scoping the requirements imposed on the processing architectures.
ADC-quantization is not sufficient for dynamic range	Artefacts in the beams and channels begin to appear. Increase the bit-depth of the ADC
Quantization of channels and equalisation	Artefacts in final images appear due to non-gaussian random noise. Increase processing bit-depths at the cost of bandwidth.
4-bit beam re-quantization is not sufficient for correlation	Artefacts in the images appear due to quantization noise. Change re-quantization to 8-bit and half the bandwidth.
Self-Induced RFI, due to station processing being close to the antennas	Data is polluted by self-generated RFI including clock signals. This can be mitigated by placing the processing chains as far away as possible from the antennas and improving the RFI-shielding.

Work until 2013

- Implement SF beamforming schemes on pathfinders
- Implement vHDL and RTL blocks for the comparison of power and performance
- Implement a tile-processor and measure results as part of AAVP
- Investigate algorithms for dense-aperture arrays, specifically in AIP and AA-mid (for example, densely packed arrays may benefit from FFT-beamforming)
- Continue imaging dynamic range simulations to evaluate beamforming performance
- Produce Design Failure mode analyses for possible architectures and technology selections