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SKA SQUARE KILOMETRE ARRAY

SKA SP CoDR: Central Beamformer Concept

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Outline

- Requirements.
- Assumptions.
- Fundamental geometry, signal processing.
- Phase-II implementation example: GSA correlator.
  - Provide general structure, w/o too much focus on chip implementation/capacity details.
- Phase-I.

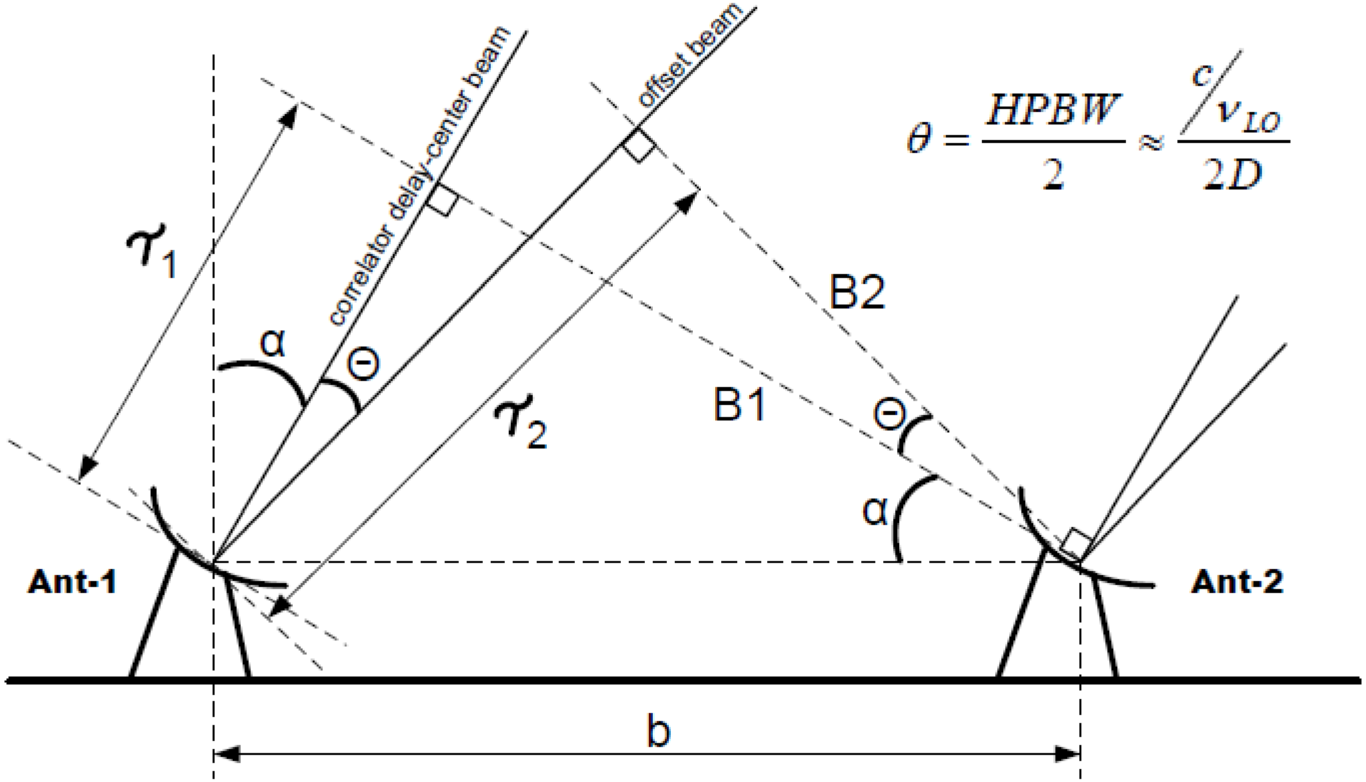
Requirements

- Phase-I: 5 km core; 35x180 m SAA stations; 175x15 m dish elements.
- Nbeams (to ~fill entire primary beam) ~= (Dcore/Delement)^2.
- SAA ~= 25 (770 possible) beams/station beam=25x480=12,000 beams; SPF ~= 111,111 beams.
- Phase-II: same 5 km core, many more elements (~165 SAA, DAA, ~1500 PAF+WBSPF). More dishes/elements for pulsar timing, but with fewer beams?
- Nbeams practically limited by cost, power, and NVP processing capacity…iteration between science requirements and technology.

Assumptions

- Coherent beams are formed.
- Delay and phase corrections are determined by correlator, and applied as beamformer coefficients.
- F-part correlator channelization is sufficient to allow for stair-step beam-offset delay tracking with phase.
- Output of beamformer is in the frequency domain, same channel resolution as the correlator (coarser channels can be produced after final sum with more DSP).
- A single serial spiggot/stream does not have to contain all channels, but multiple spiggots representing entire required bandwidth has to be able to be routed to one destination NVP.

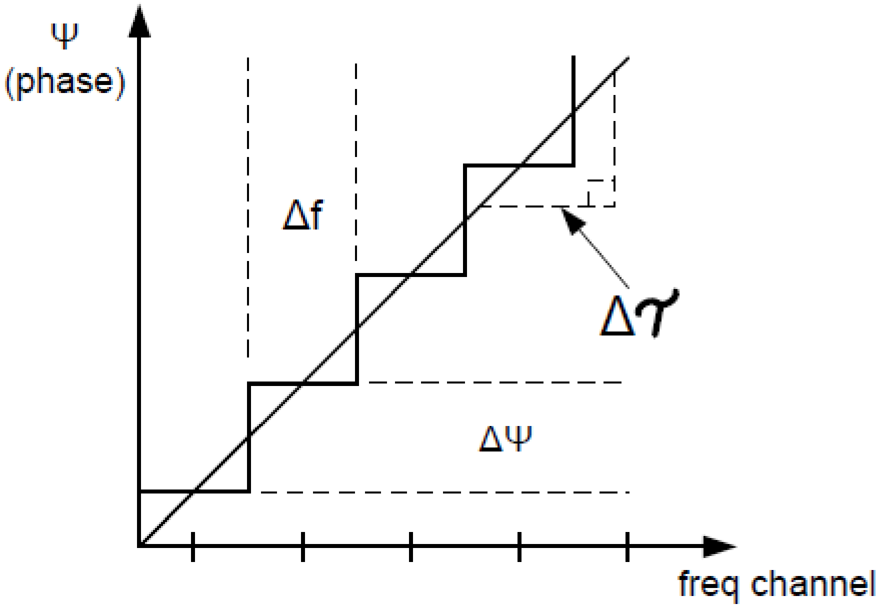
Fundamental Geometry



$$\Delta\tau = \tau_1 - \tau_2 = \frac{b}{c}\cdot[\sin(\alpha) - \sin(\alpha+\theta)]$$

$$\theta = \frac{HPBW}{2} \approx \frac{c/\nu_{LO}}{2D}$$

Fundamental Geometry



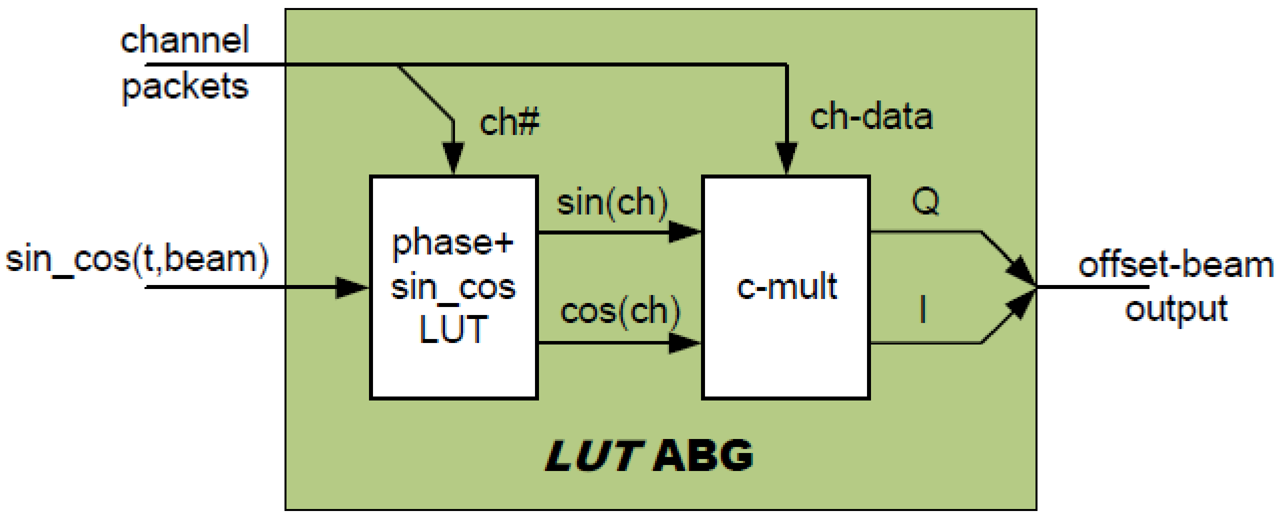
$$\Delta\psi = \Delta\tau \cdot 2\pi \cdot \Delta f$$

$$\phi_f(t) = 2\pi \cdot \Delta\tau(t) \cdot \nu_{LO}$$

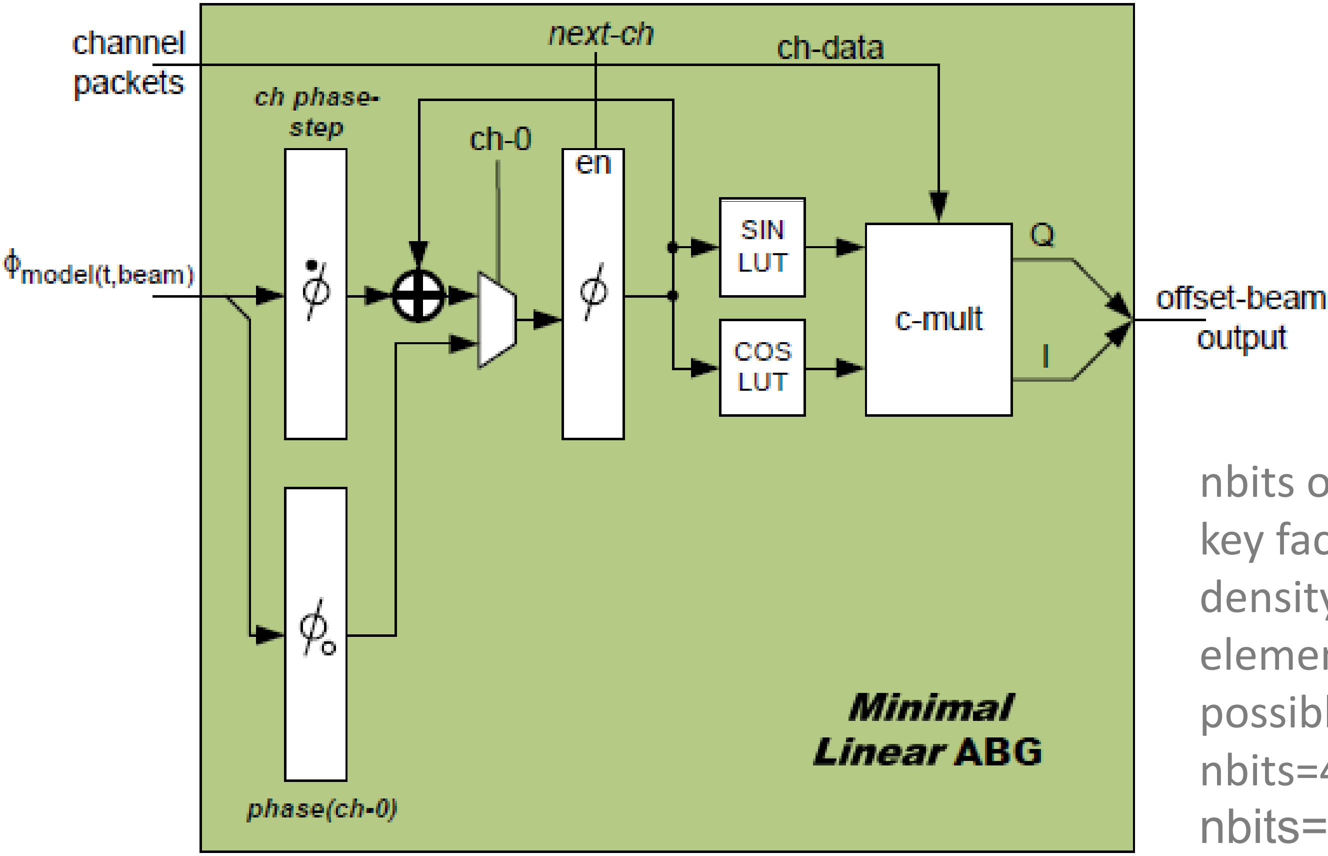
$$\eta = \frac{\sin(\Delta\psi)}{\Delta\psi}$$

Signal Processing

- For *each* element, for *each* beam, there must be an "Antenna Beam Generator" (ABG).
- Simplest form: *f* to *sin+cos* LUT, complex multiplier.
  - Could be too memory intensive, depending on number of frequency channels, but is most flexible. Coefficients are changing slowly…



Signal Processing

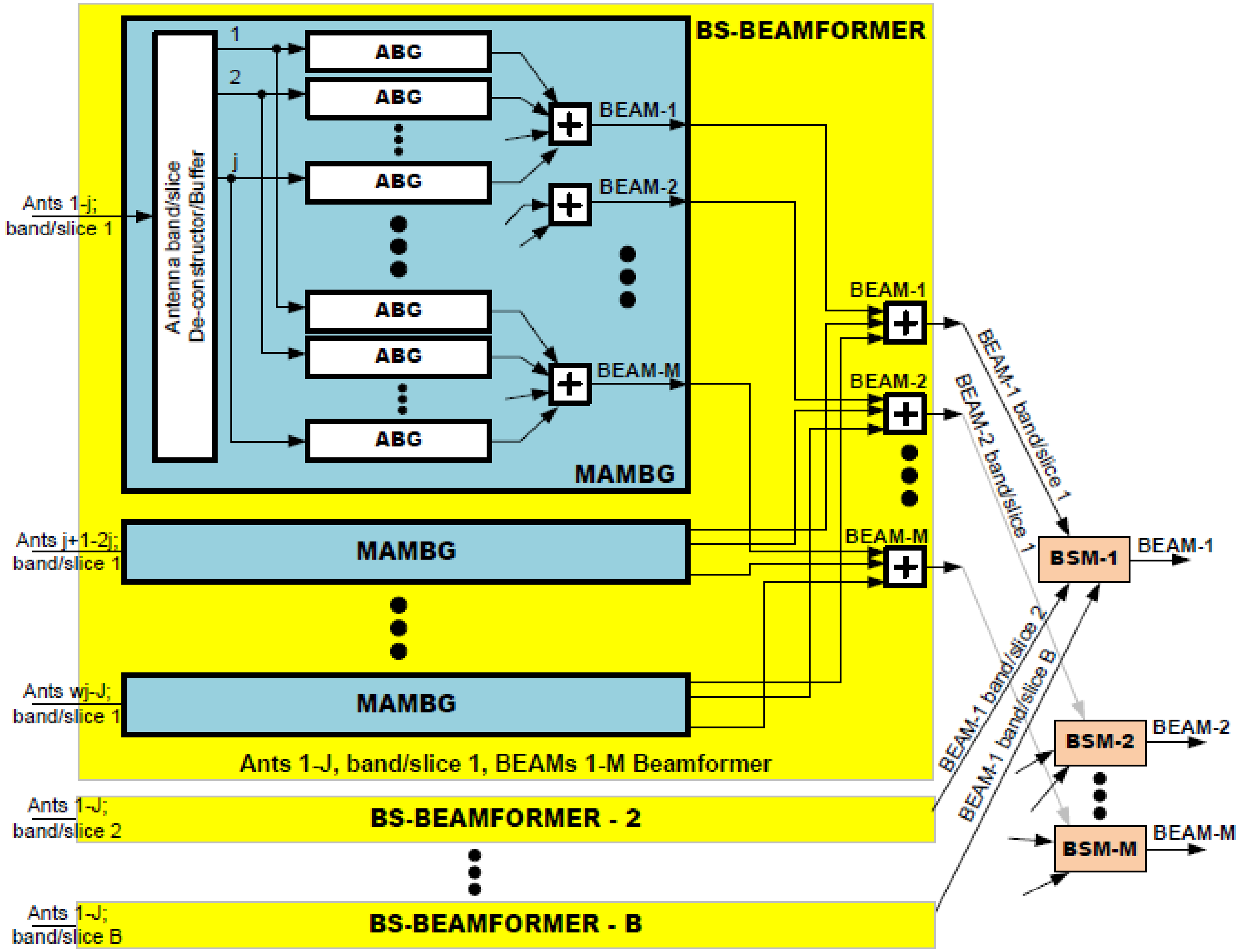


nbits out of sin/cos LUTs is key factor affecting power, density, number of elements and beams possible per chip.

nbits=4; η~=0.975

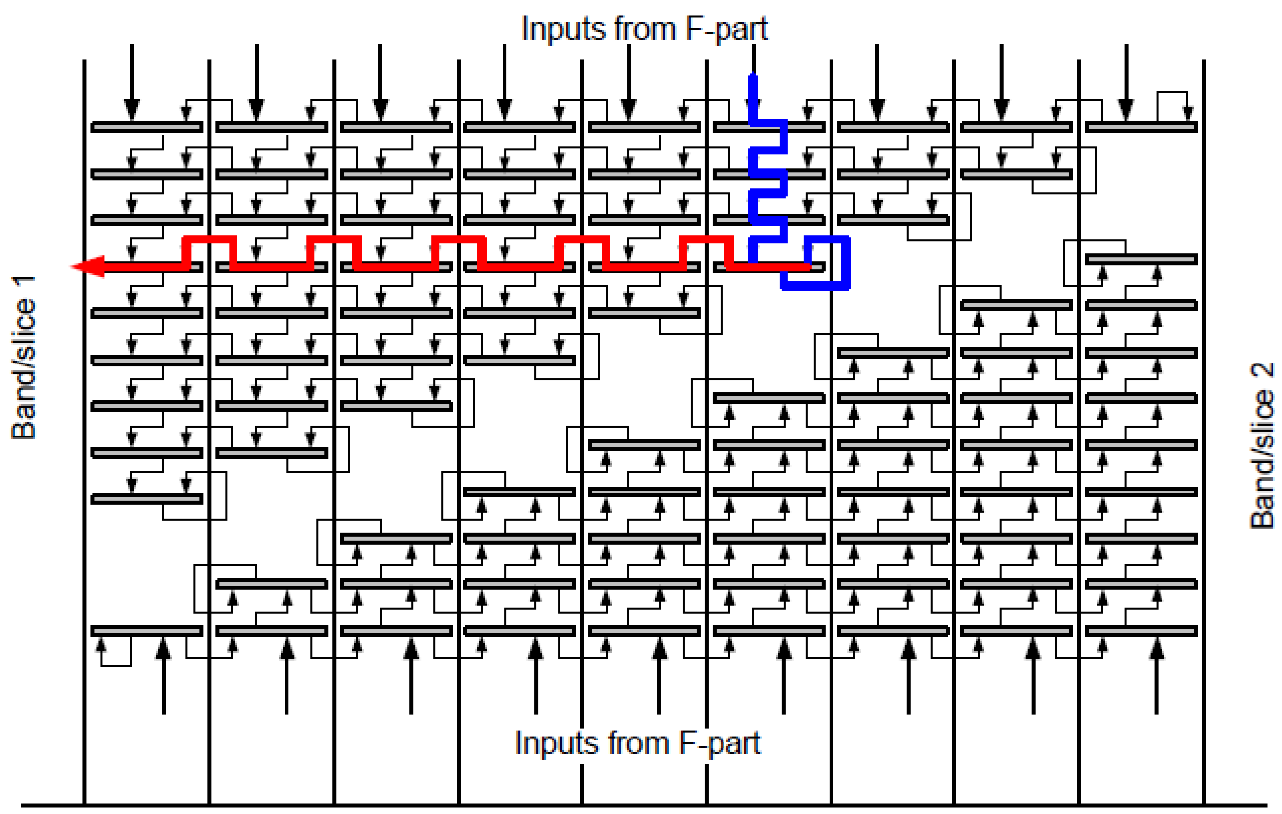
nbits=5; η~=0.9936

Signal Processing



Phase-II example: GSA

- For GSA-concept correlator, all F-part data available at ends of rack bays.

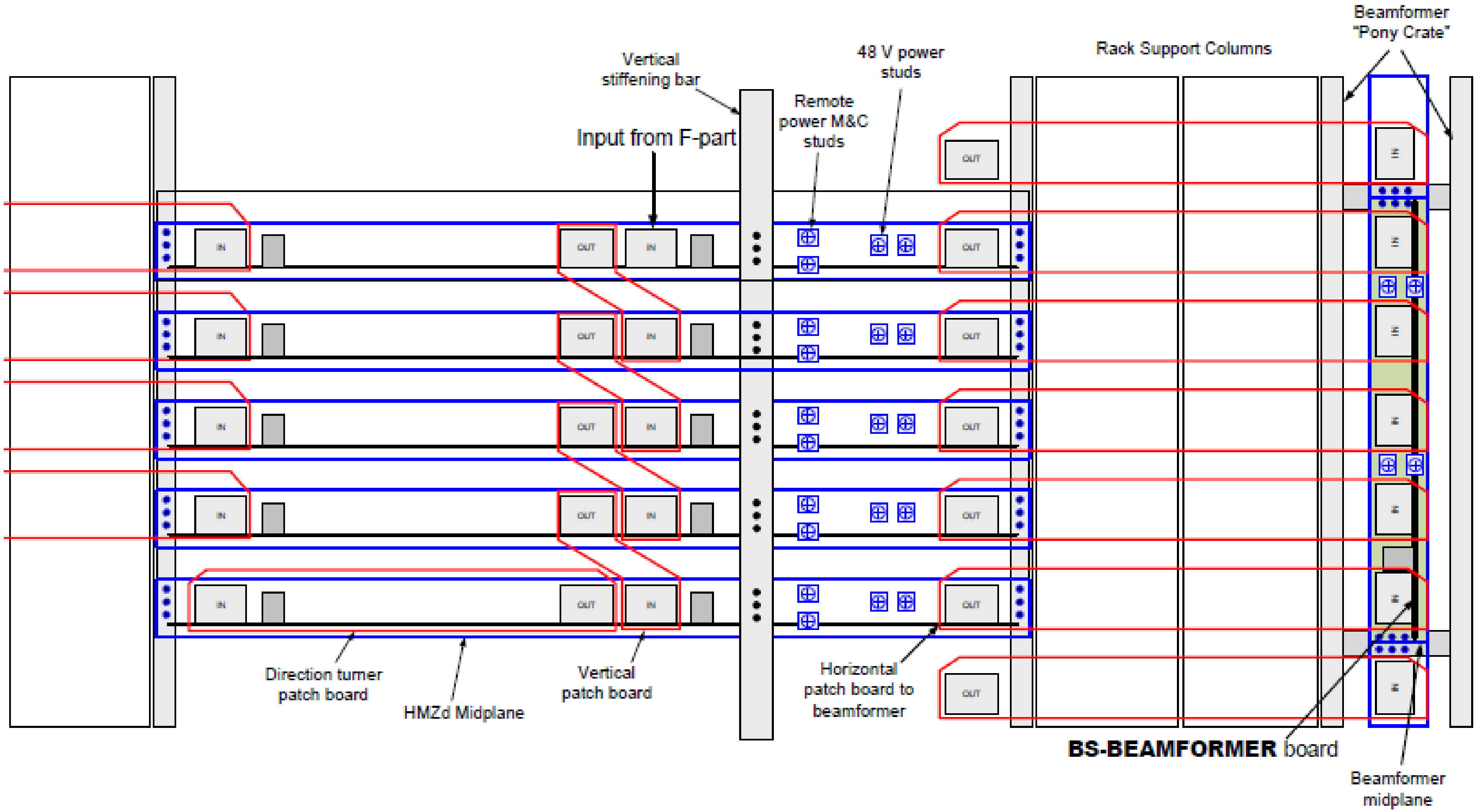


Phase-II example: GSA

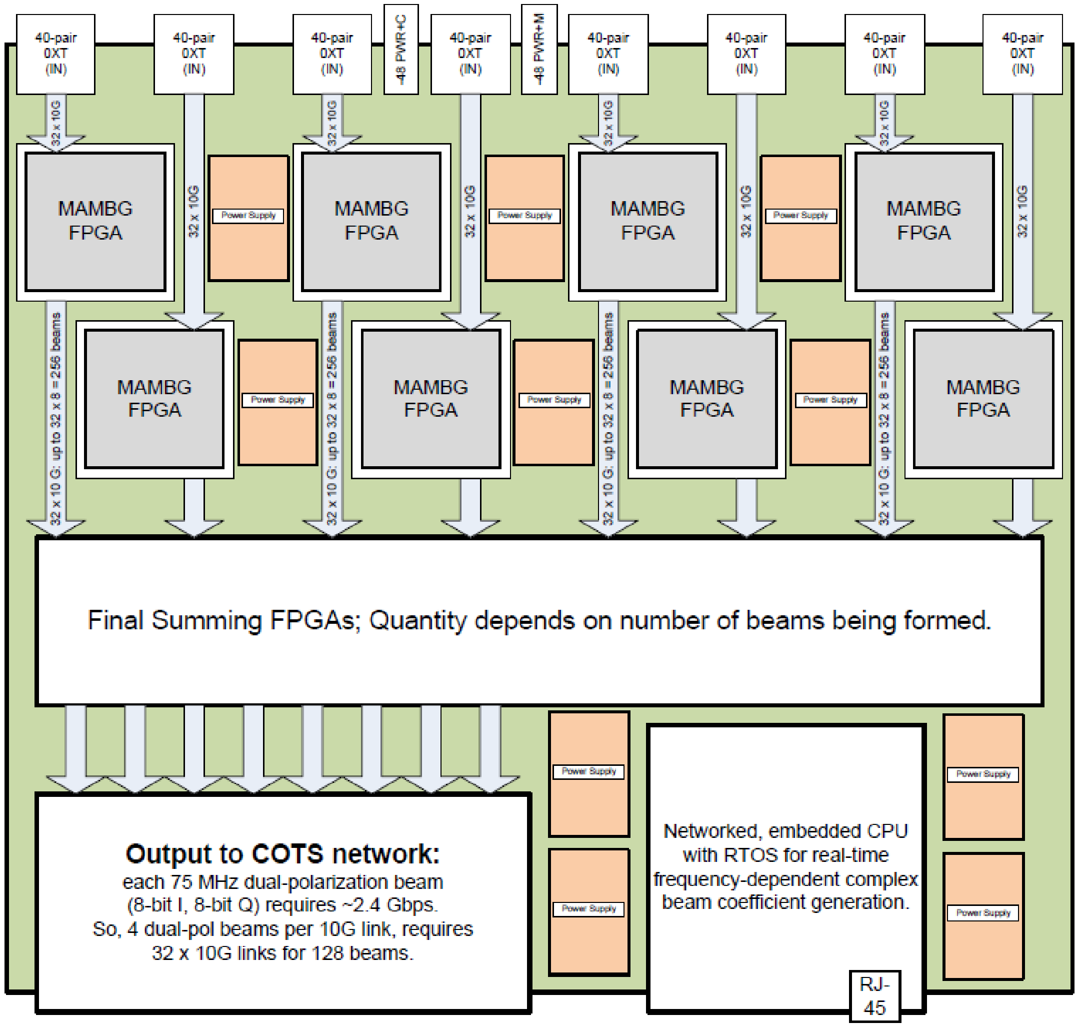
- It would be advantageous to tie into F-part data without additional cabling (fiber or otherwise), to significantly reduce cost, improve reliability etc.

- Solution: continue the daisy-chain in the same manner as used in the correlator.

Phase-II example: GSA



Phase-II example: GSA



Band/slice Beamformer Board (BSBB).

Example chip: Altera Stratix-V 5SGSD6 (2nd largest), 583k LEs, 48 Mbits RAM, 5325 9x9 multipliers (3550 18x18), 48 14G MGTs. Possibly ~12 polarized beams, 256 Ants in one device. Xilinx Virtex-7, similar capacity.

Beamformer is definitely compute dominated.

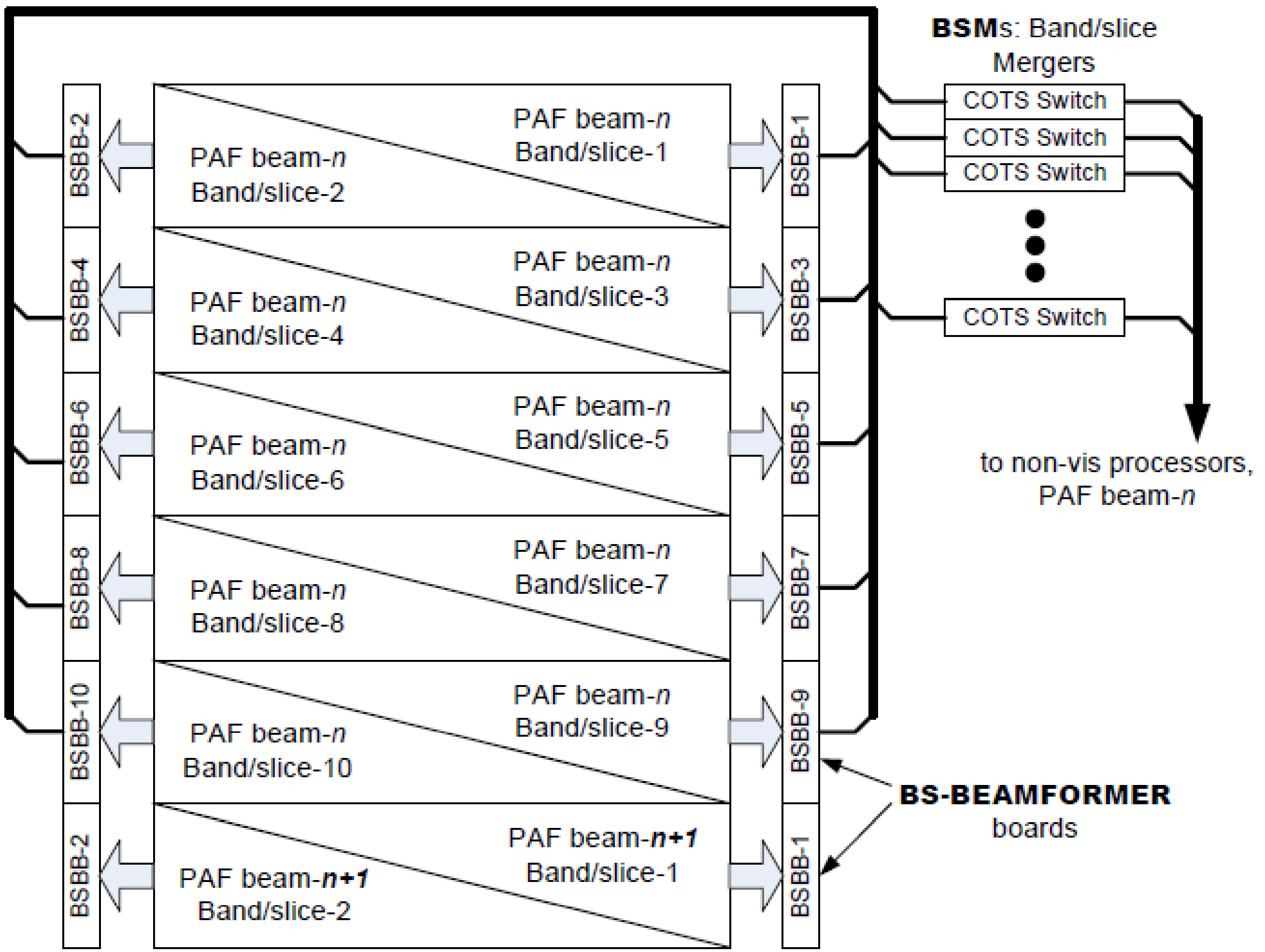
Phase-II example: GSA

- More beams anyone?

Phase-II example: GSA

- Tie all band slices together, to route single-beam, all band slices to one NVP (Band/slice Merge—BSM—function)
  - use COTS switches to perform final packet routing/merging.

Phase-II example: GSA



Phase-I

- Probably incorporate on correlator boards, or daisy-chained output of correlator boards to beamformers depending on number of beams.

- Each correlator concept has a different way of doing it…presumably will touch on Central Beamformer implementation in each correlator concept presentation.

Summary

- Must provide multiple coherent beams for central 5 km core of SKA for all receptor types.
- All operations on the F-part data output; beam-offset delay implemented as phase rotation of each channel.
- Compute rather than I/O dominated.
- Phase-II example tying into GSA F-part data; each corr concept will have different implementation.
- Phase-I closely integrated with correlator, depends on correlator implementation.