SKA SP CoDR: GSA Correlator Concept

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Outline

- Phase-II requirements.
- GSA overview.
- F-part.
- F-to-X data transport.
- X-part; baseline ASIC.
- Visibility-based addressing; gridding.
- System layout.
- Phase-I.
- Way-forward.

Phase-II Requirements

- DAAs, SAAs: 250 stations, ~1000 beams, 300-400 MHz/pol'n.
- PAF: ~2000 antennas, ~30 beams, ~700 MHz/pol'n/beam.
- WBSPF: ~3000 antennas, 1 beam, 1-n GHz/pol'n.
- ~100 kchannels/baseline/beam, possibly more at narrower bandwidths.

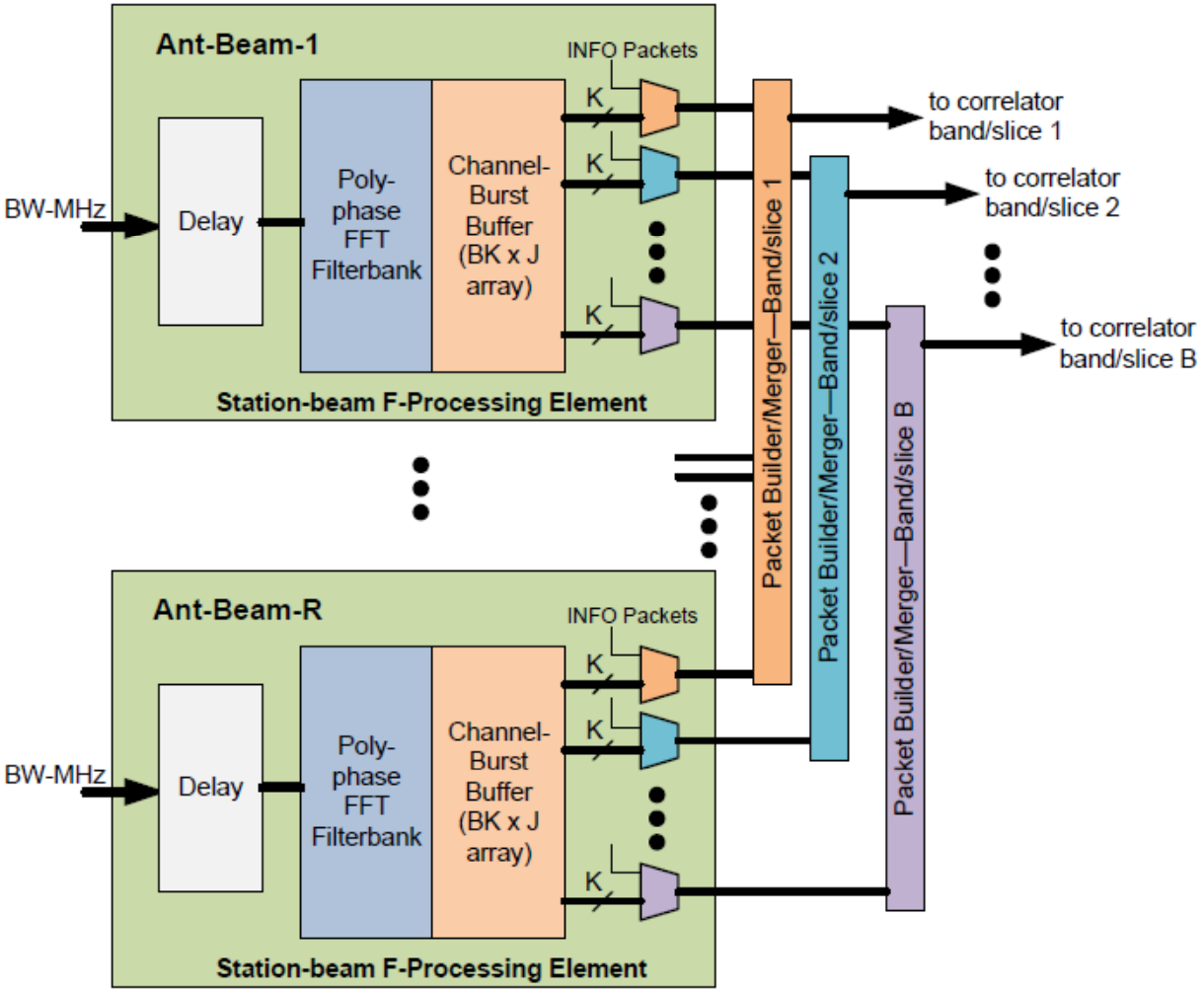
GSA Overview

- “Giant” Systolic Array.
- Physical layout to try to minimize cabling (fibers+transceivers) in the correlator, and allow for very large correlator array.
- No monolithic corner-turner required.
- Use existing and emerging technologies.
- Holistic approach—consider correlator to image processor data transport, and image processor requirements. Baseline-based integration to try to minimize bandwidth to image processors. Possibly subsume some image processing in correlator.
- Technology improvements will, of course, shrink the size of the correlator, reduce power etc.

F-part

- No detail described in CoDR document.
- Well established poly-phase FFT filter bank approach. Any correlator implementation requires this. O(N)
- Distributed partial corner turner to facilitate single-link point-to-point fiber routing to X-part.

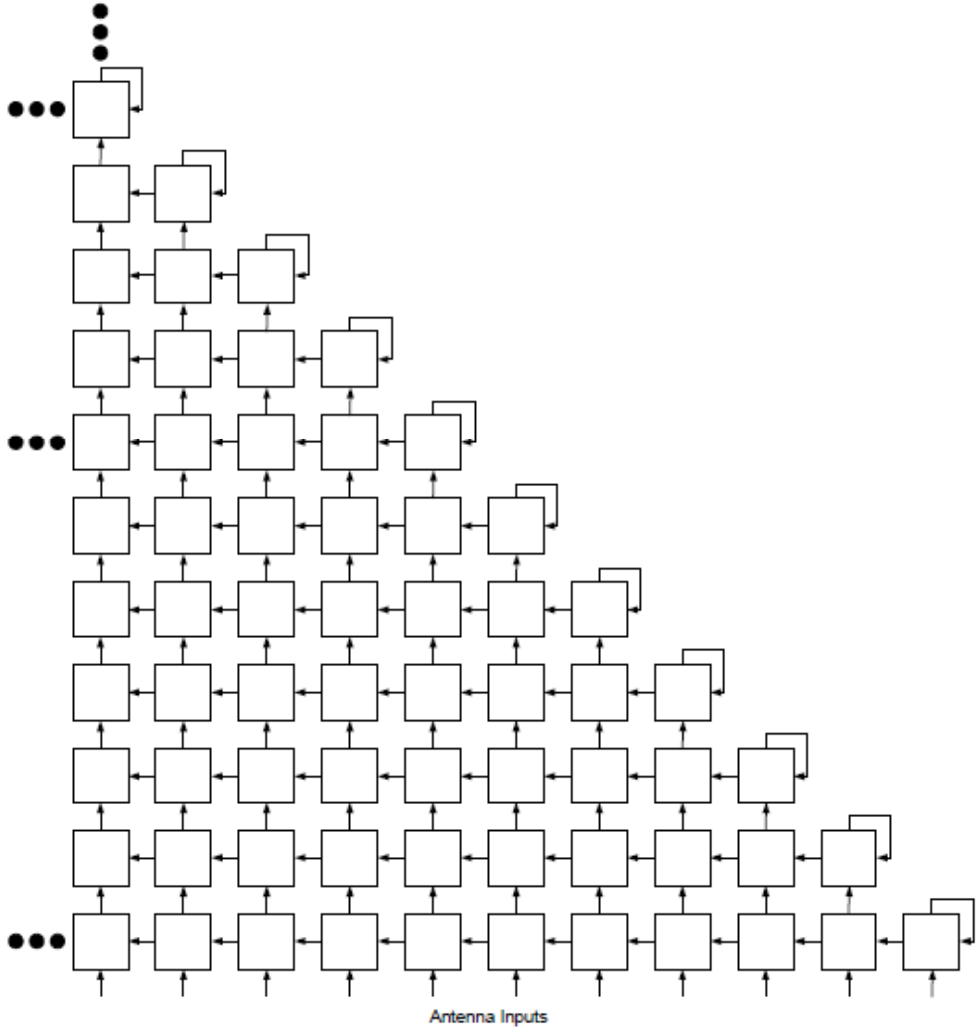
F-part


Ant-Beam-1
INFO Packets
K
K
K
BW-MHz
Delay
Poly-phase FFT Filterbank
Channel-Burst Buffer (BK x J array)
Station-beam F-Processing Element
Ant-Beam-R
INFO Packets
K
K
K
BW-MHz
Delay
Poly-phase FFT Filterbank
Channel-Burst Buffer (BK x J array)
Station-beam F-Processing Element
Packet Builder/Merger—Band/slice 1
Packet Builder/Merger—Band/slice 2
Packet Builder/Merger—Band/slice B
to correlator band/slice 1
to correlator band/slice 2
to correlator band/slice B

F-to-X Data Transport

- Single link, point-to-point.
  - F-part of the correlator *could* be somewhere else…
- Might use short-range, high-density fiber connections; SNAP12 with F-end multi-fiber breakout?
  - Details TBD.
- Each fiber has single “insertion point” into the correlator.

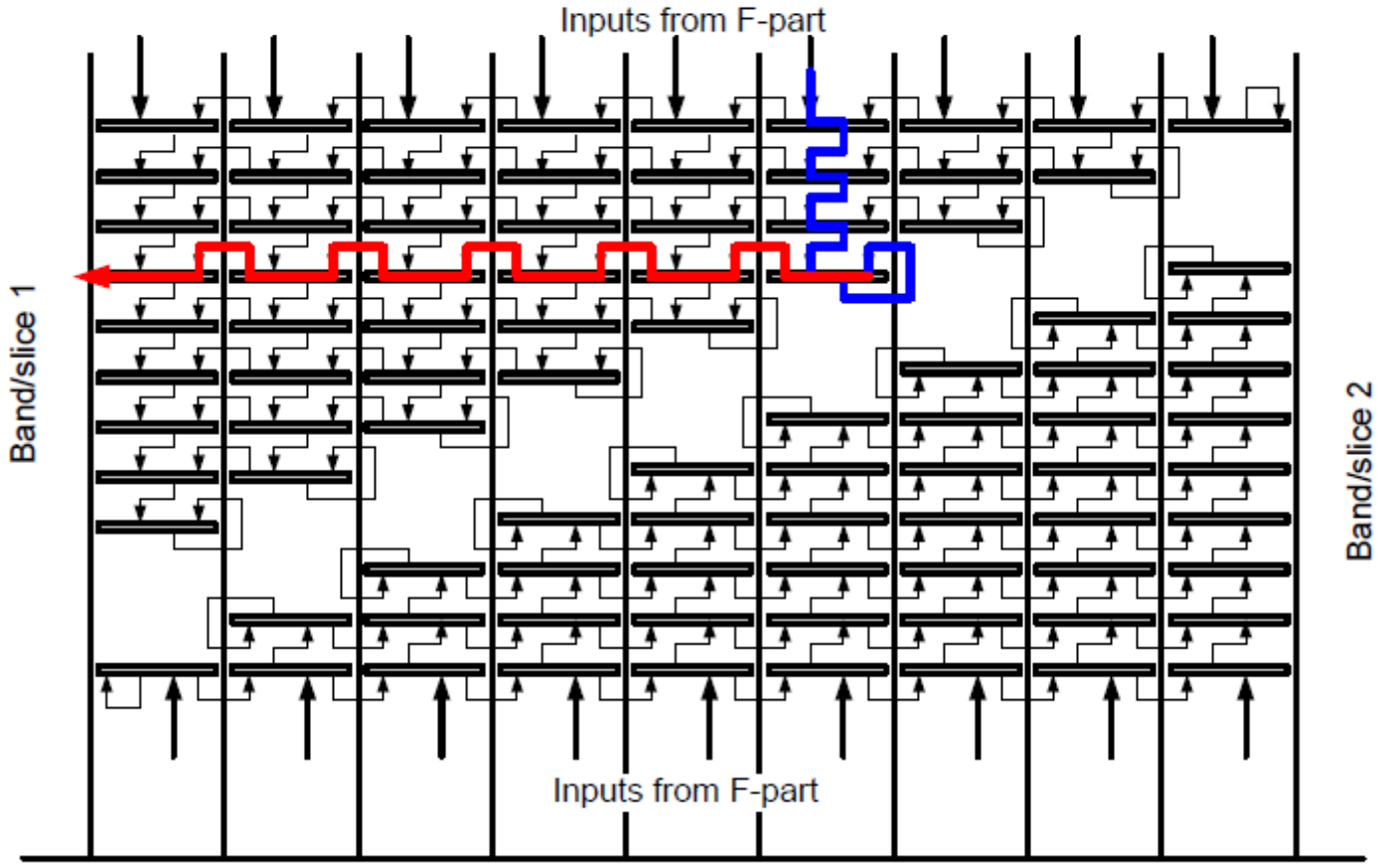
X-part



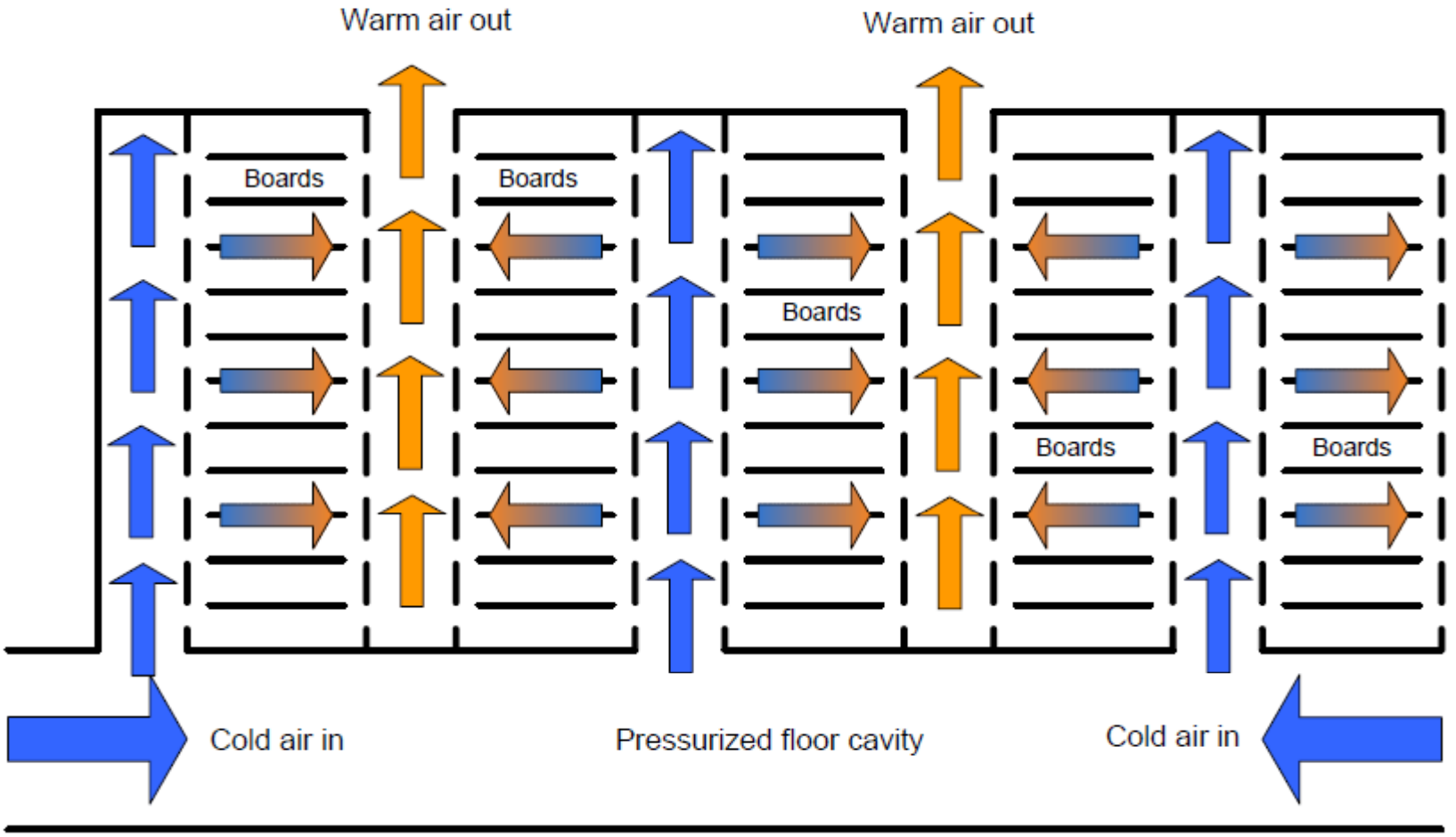
X-part

- Mount boards horizontally.
- Establish nearest neighbour connections with printed wiring “patch boards”. Easy+fast to install, reliable, low-cost. Cu interconnects, no fiber+transceivers.
- Problems?
  - Higher precision rack mechanics.
  - How to cool?

X-part


Inputs from F-part
Band/slice 1
Band/slice 2
Inputs from F-part

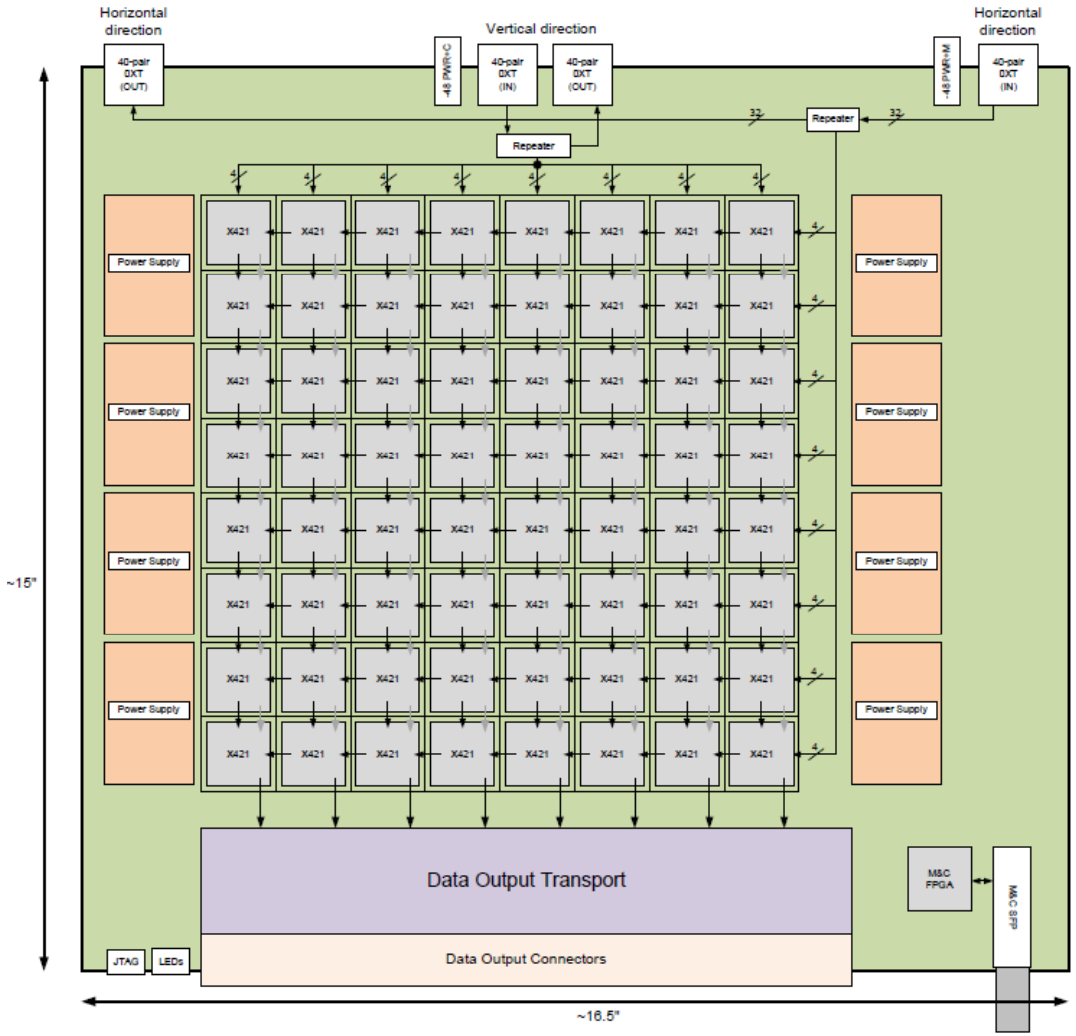
X-part


Warm air out
Warm air out
Boards
Boards
Boards
Boards
Boards
Cold air in
Pressurized floor cavity
Cold air in

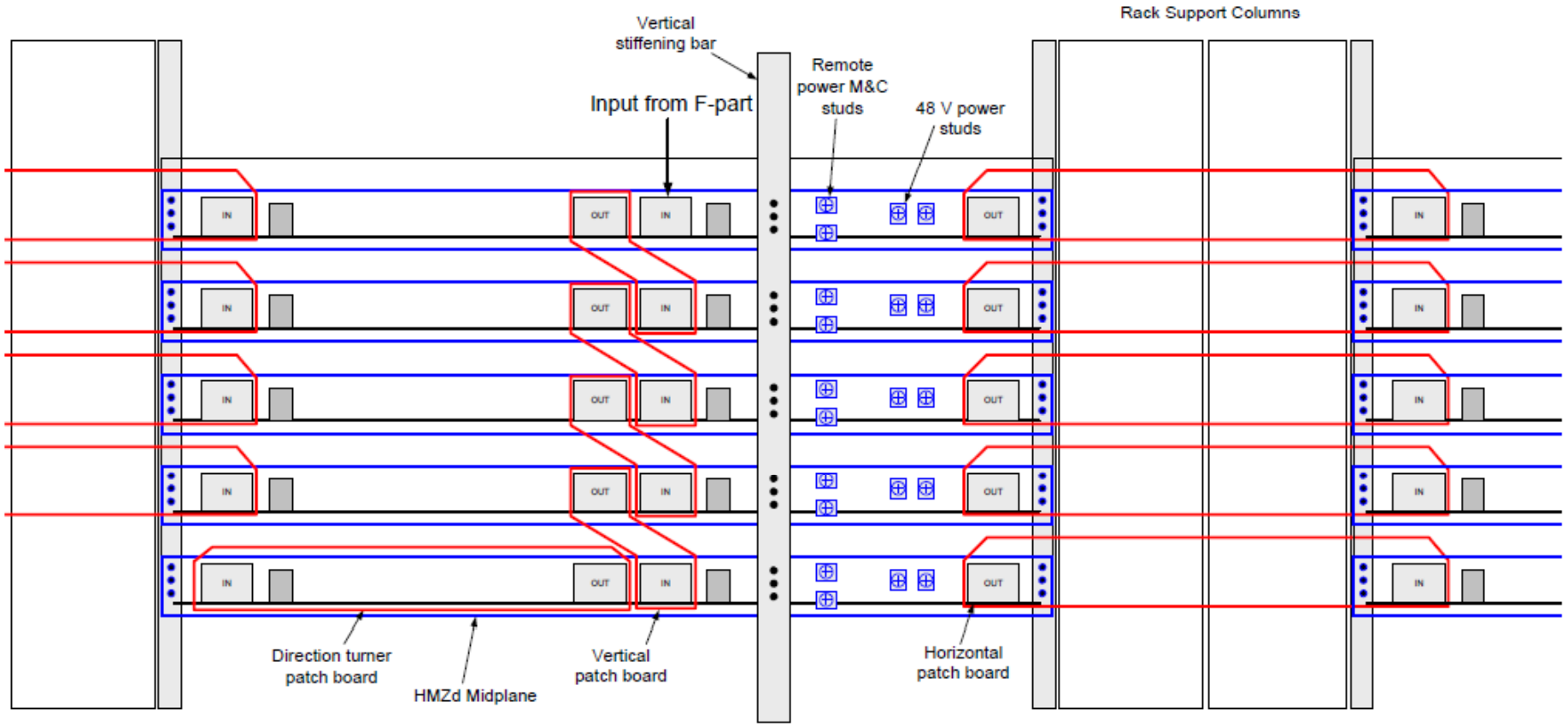
X-part

- Correlator board:
  - ~8x8 array of ASICs. Use ASICs with on-chip eDRAM for low power, minimal I/O connections for yield and reliability.
    - Larger/fewer chips might save power.
  - use SERDES for all I/O (minimal solder contacts).
  - Make as simple as possible to maximize production yield and reliability.

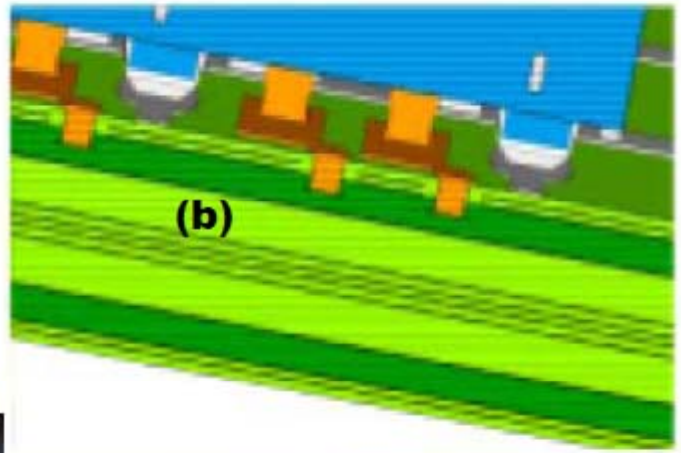
X-part

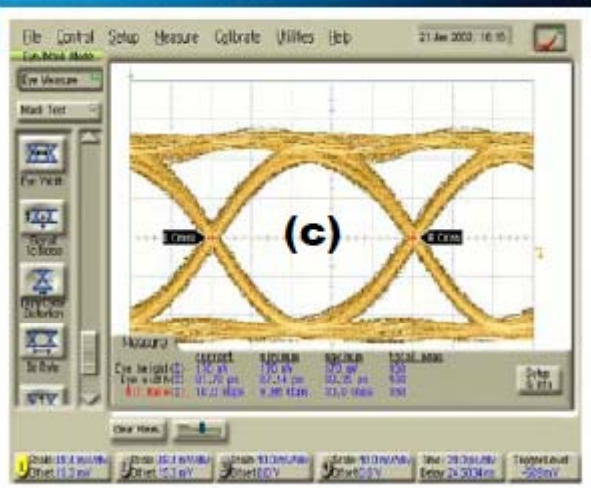

Horizontal direction
Vertical direction
Horizontal direction
40-pair DXT (OUT)
48 PWR+C
40-pair DXT (IN)
40-pair DXT (OUT)
48 PWR+M
40-pair DXT (IN)
Repeater
Repeater
32
32
4
X421
Power Supply
Data Output Transport
Data Output Connectors
M&C FPGA
M&C SFP
JTAG
LEDs
~15"
~16.5"

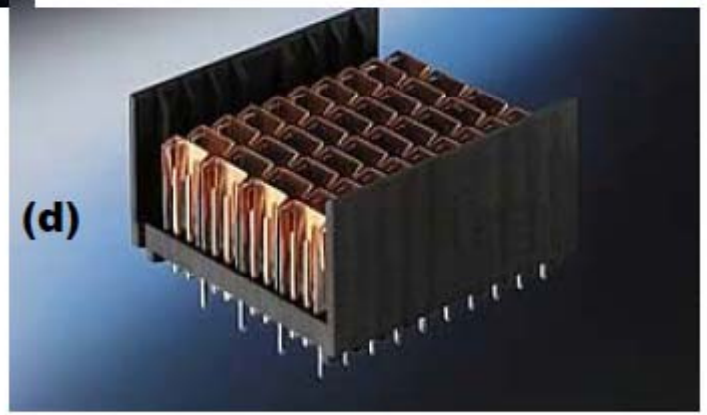
X-part


Vertical
stiffening bar
Input from F-part
Remote
power M&C
studs
48 V power
studs
Rack Support Columns
IN
OUT
Direction turner
patch board
HMZd Midplane
Vertical
patch board
Horizontal
patch board

X-part





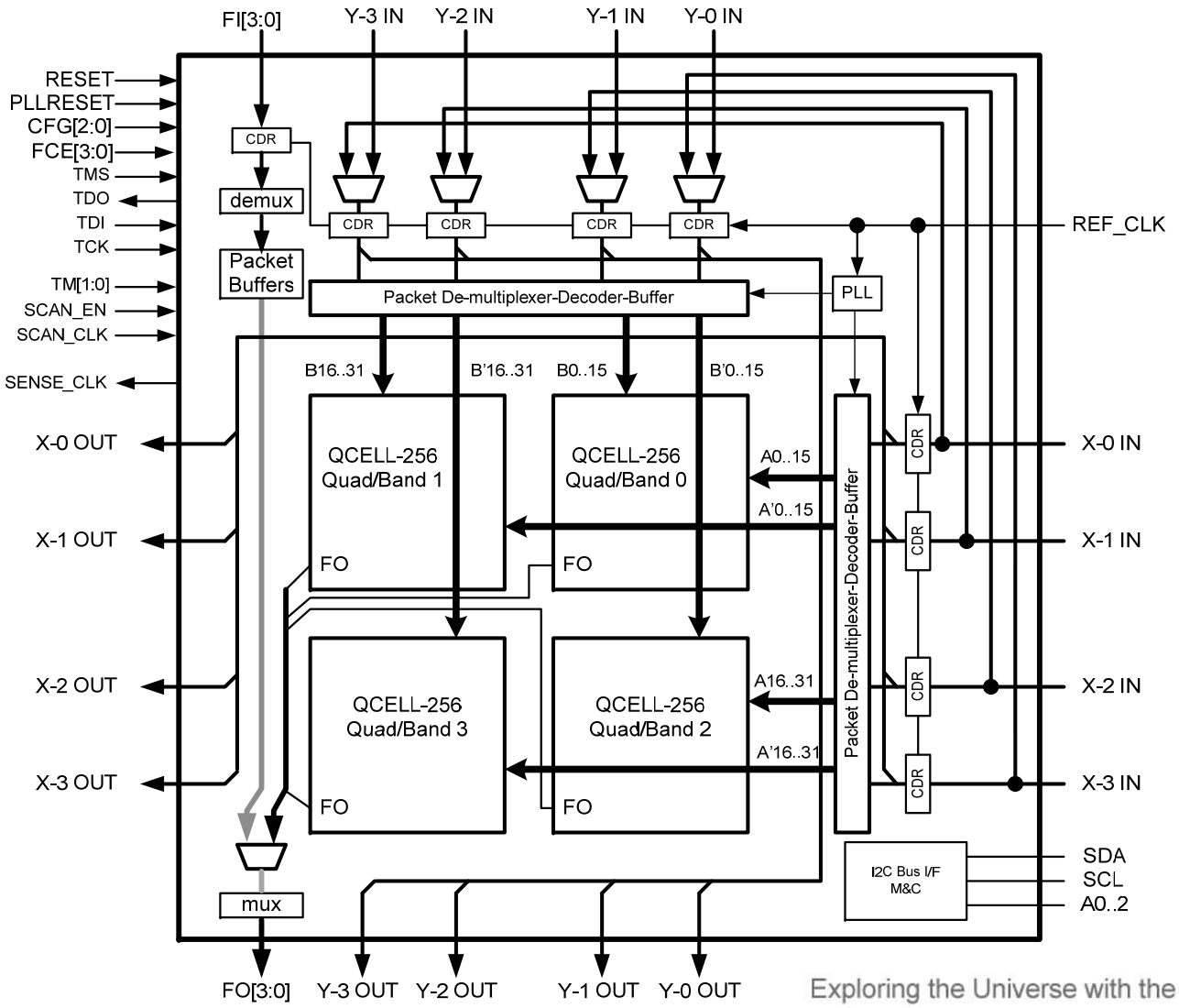


0XT connector

X-part

- "X421" baseline ASIC concept.
  - 1024 baseline, 4+4-bit, 2048 channel/product, 75 MHz/pol'n.
  - Baseline-based integration.
  - Baseline u,v,w calculation + "INFO" to provide image processors with required information for r.t. imaging.
  - Per-channel data valid flagging/counting for temporal per-channel RFI excision.
  - I2C for minimal M&C I/O.
  - Internal clock rate, 312.5 MHz…could be more ambitious.
  - Design to allow for use in SAA, DAA single-board all ants correlation.
  - 8 ants multiplexed onto each 10G link.

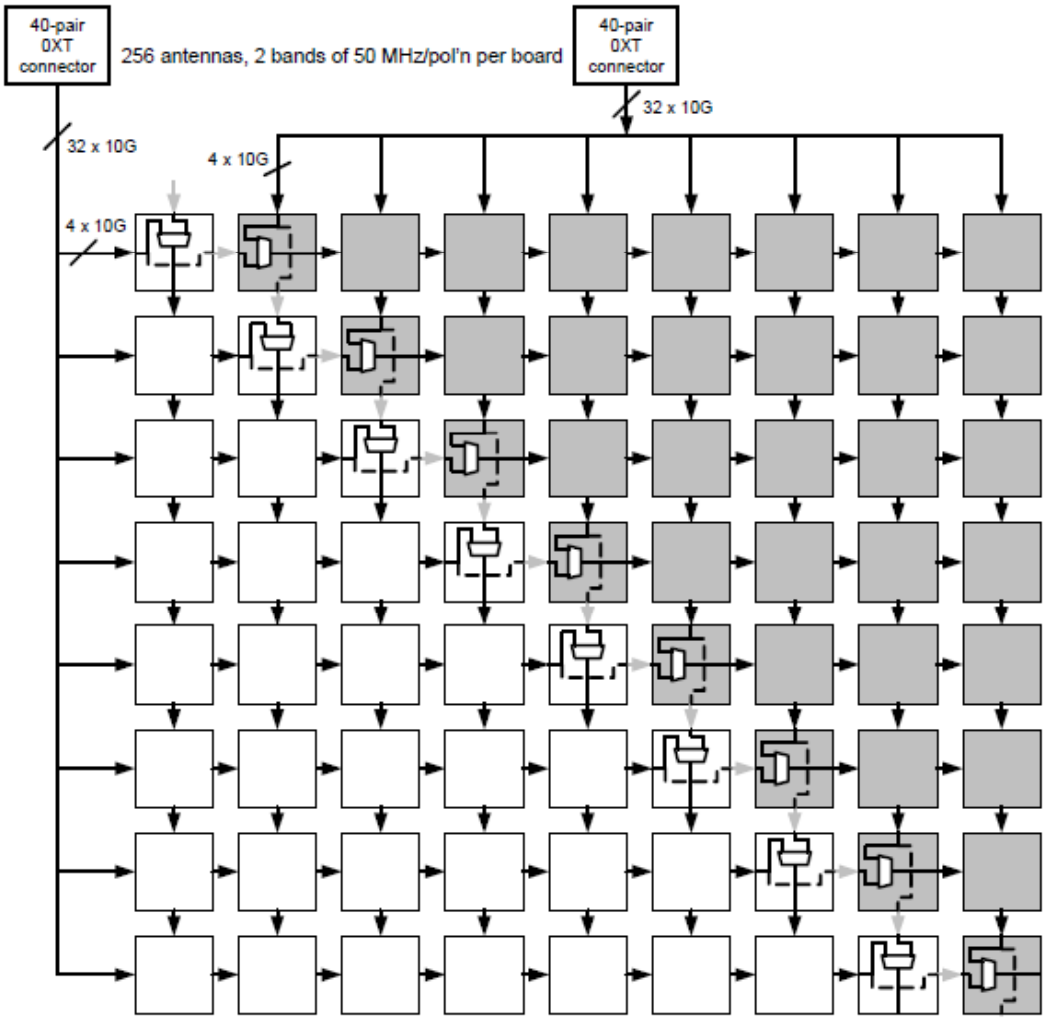
X-part


FI[3:0]
Y-3 IN
Y-2 IN
Y-1 IN
Y-0 IN
RESET
PLLRESET
CFG[2:0]
FCE[3:0]
TMS
TDO
TDI
TCK
TM[1:0]
SCAN_EN
SCAN_CLK
SENSE_CLK
X-0 OUT
X-1 OUT
X-2 OUT
X-3 OUT
CDR
demux
Packet Buffers
mux
FO[3:0]
Y-3 OUT
Y-2 OUT
Y-1 OUT
Y-0 OUT
REF_CLK
PLL
Packet De-multiplexer-Decoder-Buffer
B16..31
B'16..31
B0..15
B'0..15
QCELL-256 Quad/Band 1
QCELL-256 Quad/Band 0
QCELL-256 Quad/Band 3
QCELL-256 Quad/Band 2
FO
A0..15
A'0..15
A16..31
A'16..31
Packet De-multiplexer-Decoder-Buffer
X-0 IN
X-1 IN
X-2 IN
X-3 IN
I2C Bus I/F M&C
SDA
SCL
A0..2

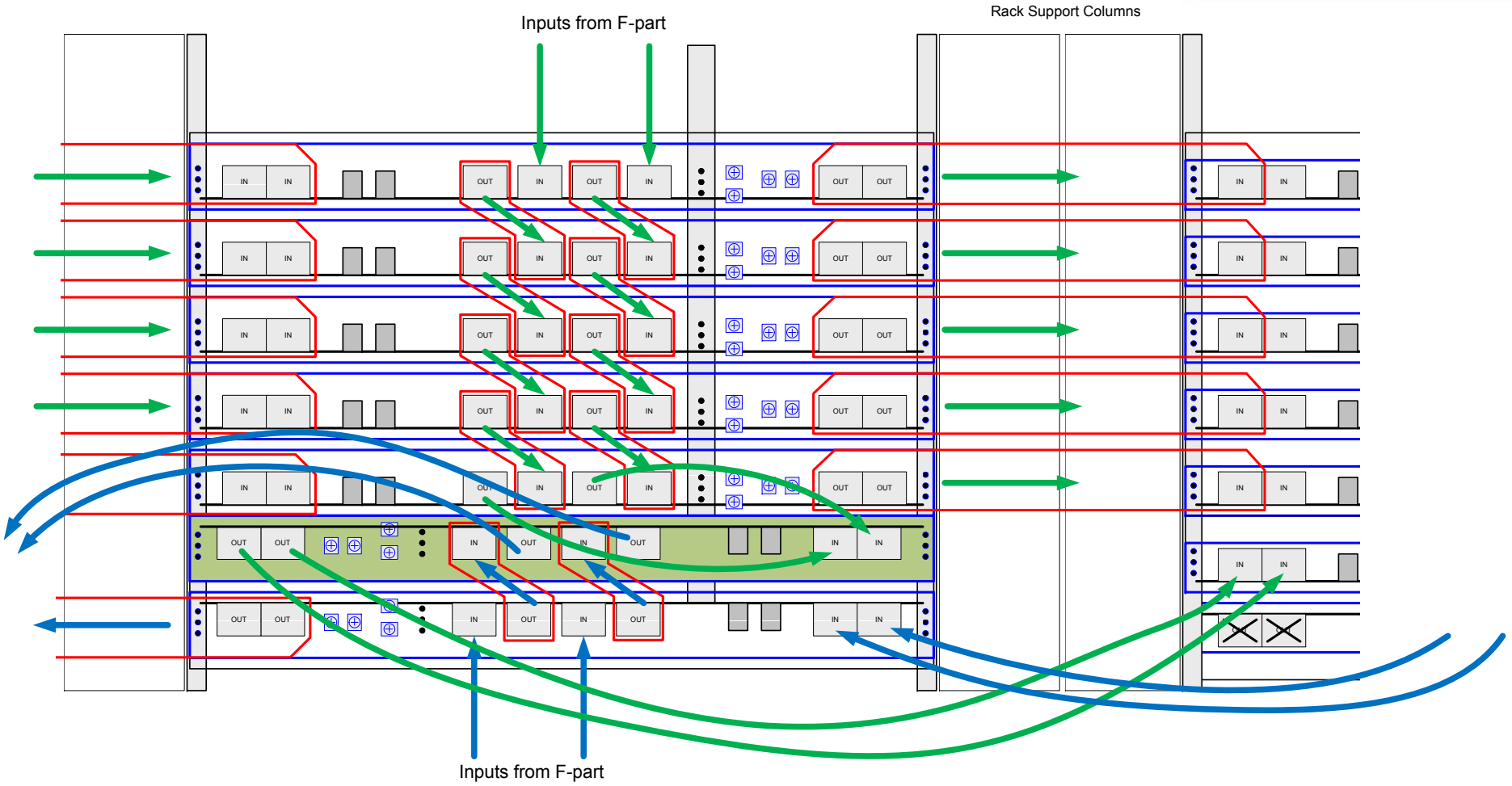
X-part

- Better board design to allow for SAA, DAA single-board band/slice correlations.
- 9x8 chips…if ASIC design can split into 2 Δ's, then 8x8 chips.
- Allows adjacent band/slice correlators to share boards…saves boards.

X-part


40-pair
0XT
connector
256 antennas, 2 bands of 50 MHz/pol'n per board
40-pair
0XT
connector
32 x 10G
32 x 10G
4 x 10G
4 x 10G

X-part



X-part

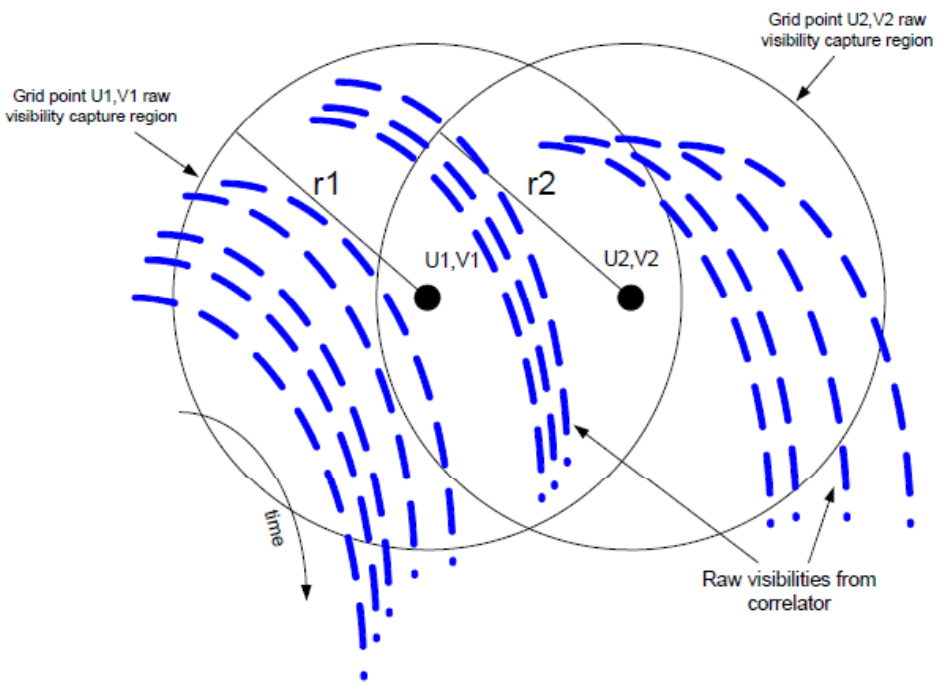
- Of course, with more ants per 10G, and/or larger ASIC capacity, the *need* for horizontal board mounting disappears at some point, as all boards for a band/slice can fit in one crate.

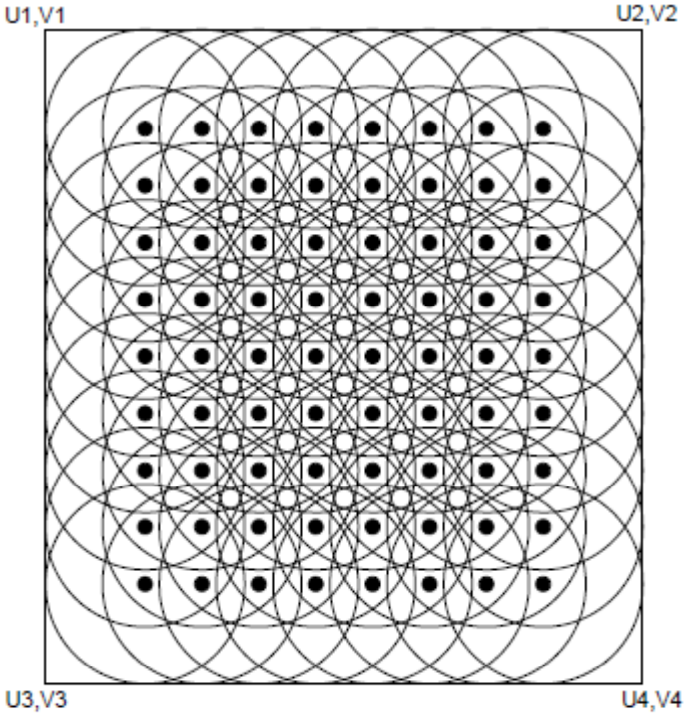
VBA

- VBA—Visibility-Based Addressing.

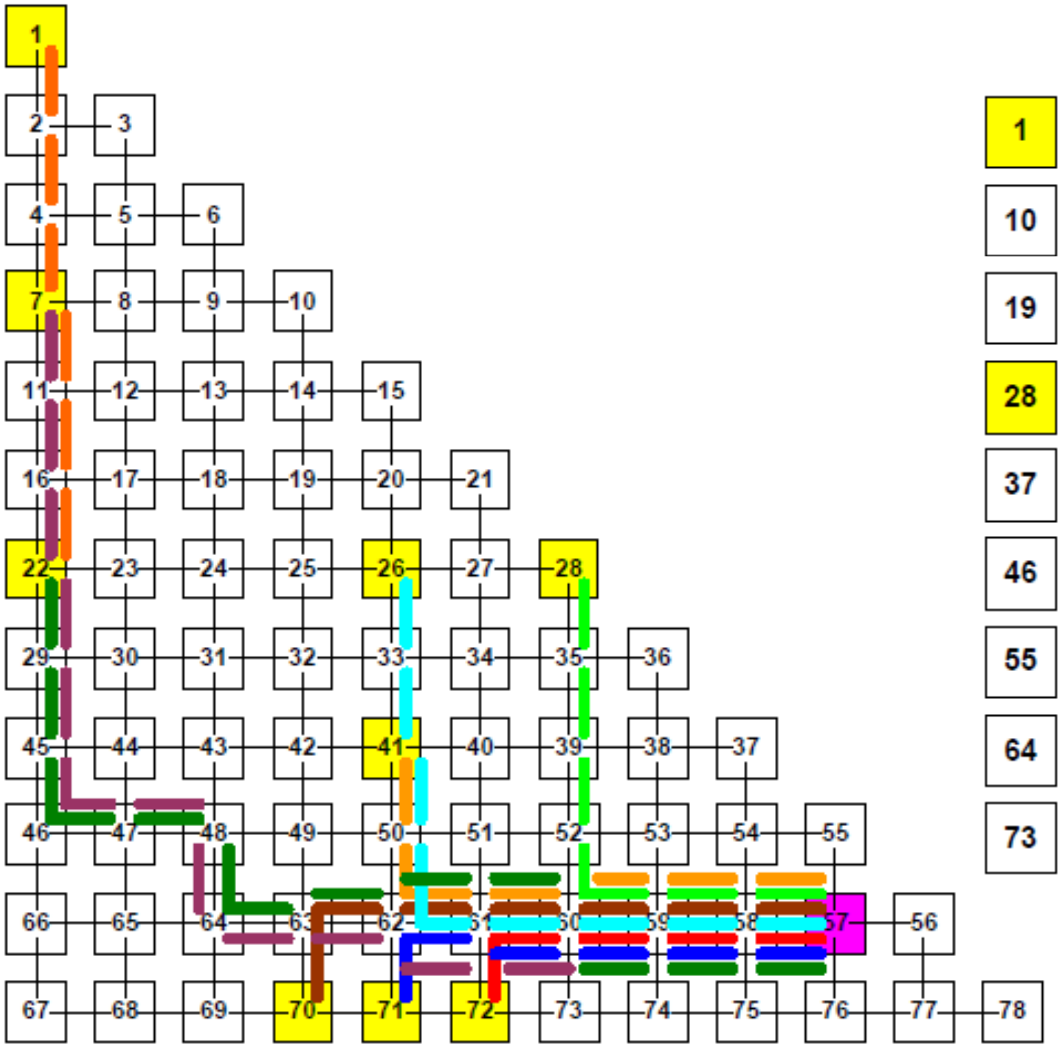
- Try to get the correlator to “collate” data so each image processor (gridder) gets only the data it needs.
  - ASIC calculates baseline visibilities, includes in output frame.
  - Route packets within correlator nearest-neighbour network.
  - Point-to-point correlator to gridding CPU connections…no worries about switch packet collisions/bottlenecks.

VBA


Grid point U1,V1 raw visibility capture region
Grid point U2,V2 raw visibility capture region
r1
r2
U1,V1
U2,V2
time
Raw visibilities from correlator

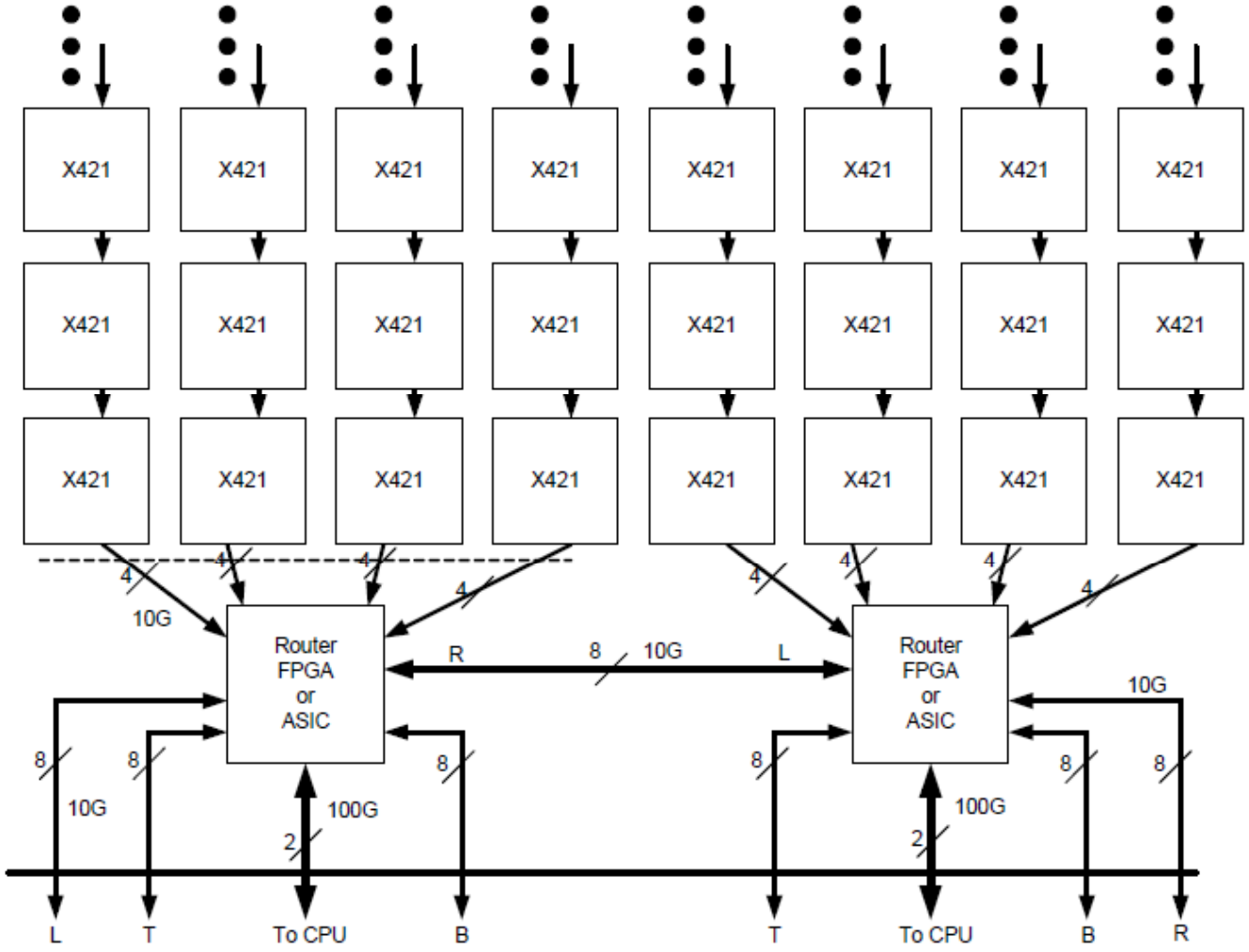

U1,V1
U2,V2
U3,V3
U4,V4

VBA

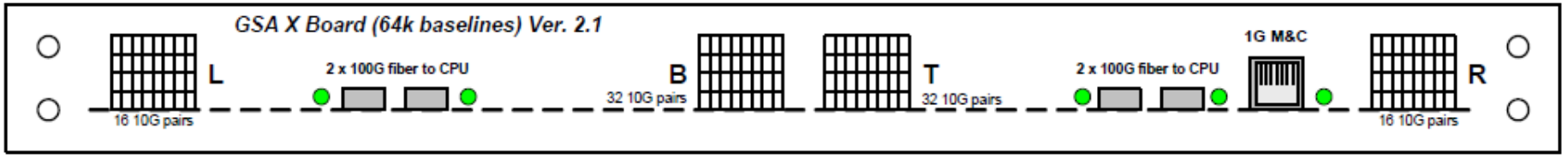


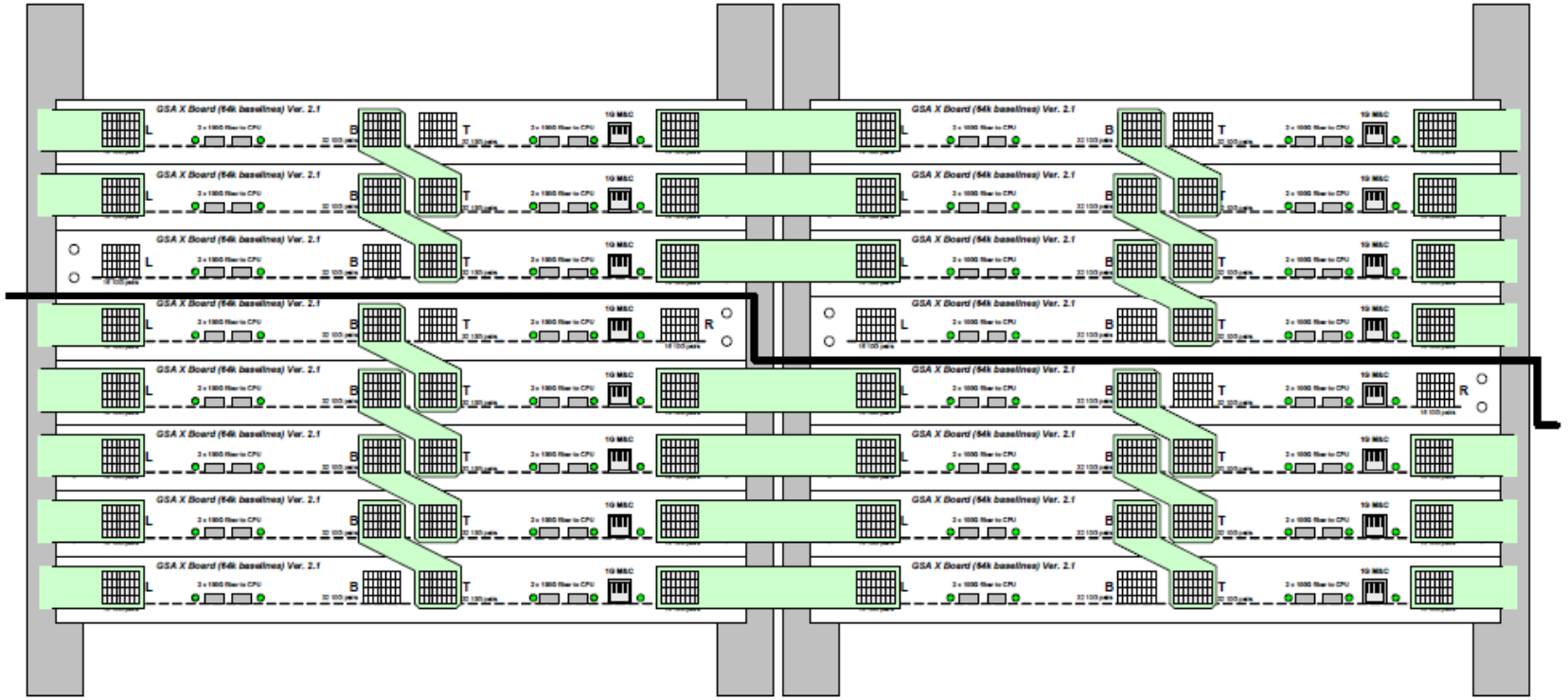
1	2	3	4	5	6	7	8	9
10	11	12	13	14	15	16	17	18
19	20	21	22	23	24	25	26	27
28	29	30	31	32	33	34	35	36
37	38	39	40	41	42	43	44	45
46	47	48	49	50	51	52	53	54
55	56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71	72
73	74	75	76	77	78	79	80	81

VBA



VBA

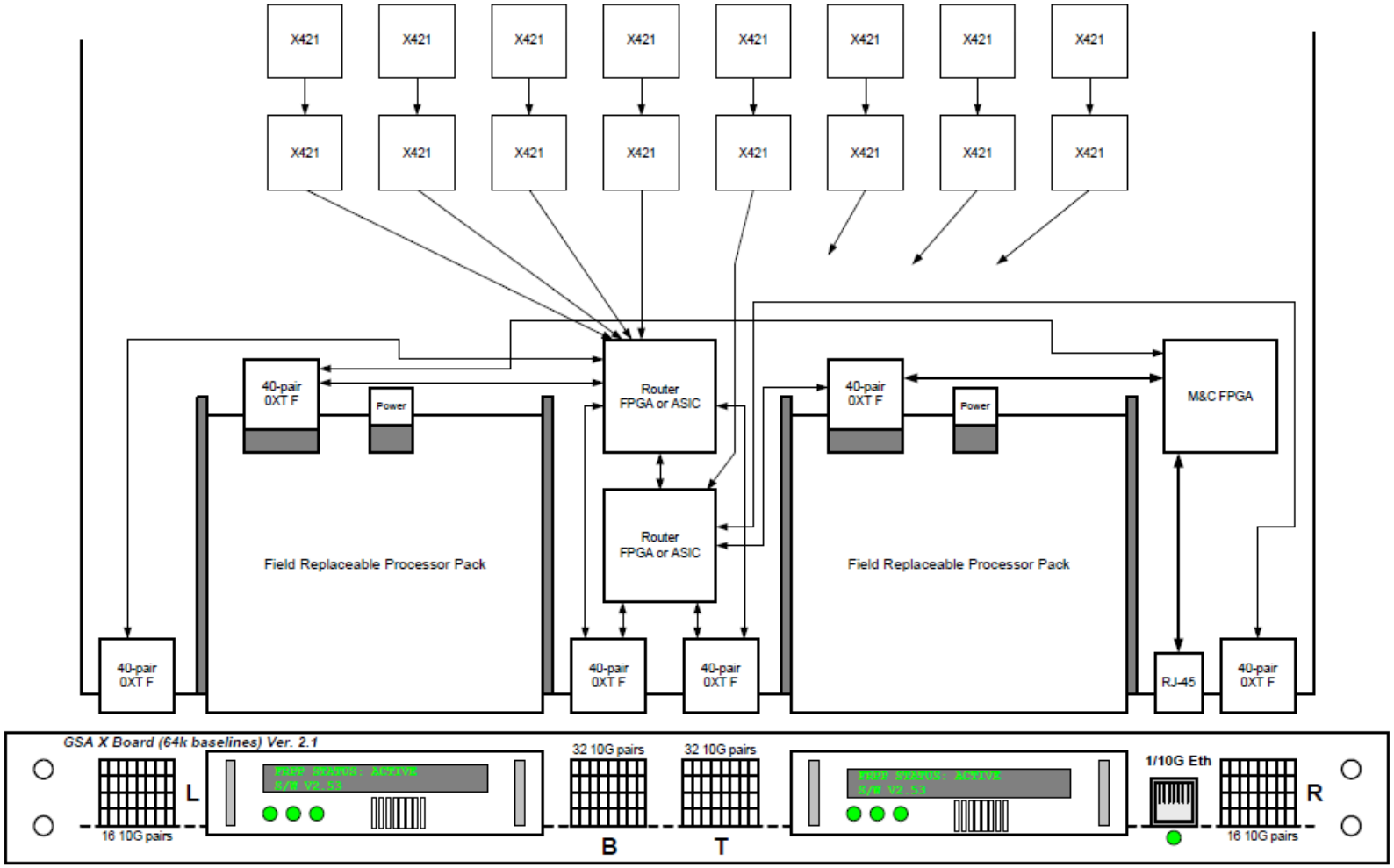

GSA X Board (64k baselines) Ver. 2.1
L
2 x 100G fiber to CPU
16 10G pairs
B
32 10G pairs
T
32 10G pairs
2 x 100G fiber to CPU
1G M&C
R
16 10G pairs



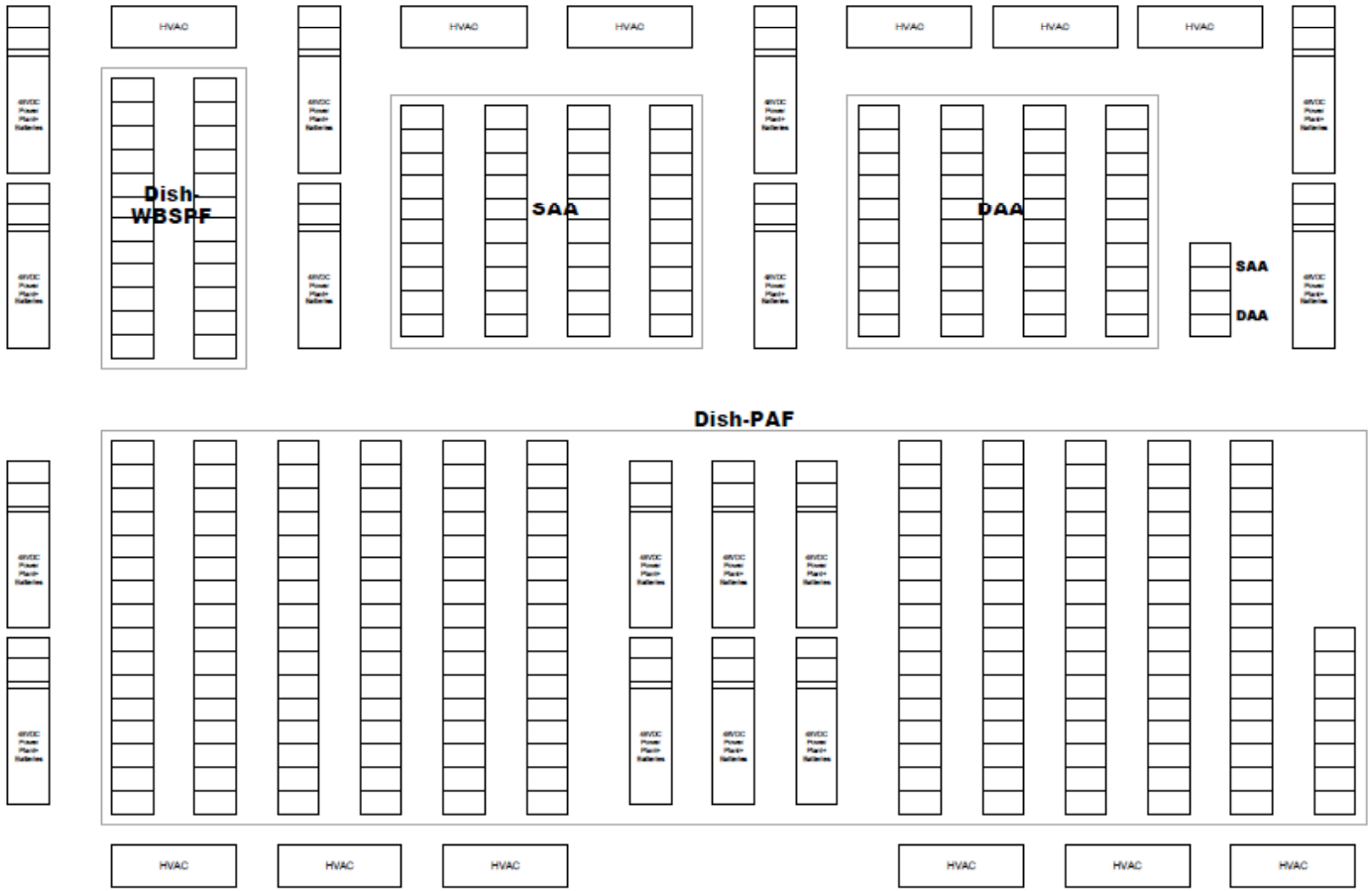
VBA

- Still a lot of data and fiber connections coming out of the correlator!
- Possibly subsume the gridding CPUs into the correlator, to minimize correlator output bandwidth.
  - Low-power high-performance CPUs…possibly tailored just for gridding?

VBA


X421
X421
X421
X421
X421
X421
X421
X421
X421
X421
X421
X421
X421
X421
X421
X421
40-pair
0XT F
Power
Router
FPGA or ASIC
40-pair
0XT F
Power
M&C FPGA
Router
FPGA or ASIC
Field Replaceable Processor Pack
Field Replaceable Processor Pack
40-pair
0XT F
40-pair
0XT F
40-pair
0XT F
RJ-45
40-pair
0XT F
GSA X Board (64k baselines) Ver. 2.1
L
16 10G pairs
32 10G pairs
32 10G pairs
B
T
1/10G Eth
R
16 10G pairs

System Layout



~34 x 22 m
Not F-part, but includes embedded gridding CPUs.
Cost: ~$200M
Power: ~7.8 MW.

Phase-I

- Tiny in comparison to full SKA (for dishes, anyway).
- GSA not good fit…see CoDR doc.
- Probably better to use FPGA boards.
- We are developing the "**Kermode**" ATCA 8 TMAC/s multi-FPGA card, which could be used as follows (assume 8-bit sampling, 4+4b correlation):

Phase-I

- Dishes (1 GHz/pol'n, 250 elements).
  - 800 MHz/pol'n, 2, possibly 3 crates.
  - Next gen ("**Kermode-2**"): 1 GHz/pol'n, 1 crate.
- SAAs (380 MHz/pol'n, 50 elements, 480 beams).
  - 60 crates (30 racks); 8 beams, 64 stations/crate.
- SAA beamformer (700 analog-BF-elements)
  - 3 crates—FFT+XConnect + 4-6 crates for BF.

Way forward

- What we do regarding Phase-II depends on funding/implementation timeline.
- CoDR doc has Gantt chart if it were actually a project…
- But if we did something now, here's how it might go leading up to the PDR…

Way forward

- X421 ASIC design study.
  - Provides baseline numbers in ~2018 technology.
- Rack mechanics/thermodynamics design.
- Correlator board preliminary layout, SI-eye modelling/testing.
- Correlator-to-gridder algorithm dev+test.
  - iterate with I.P. types.

Way forward

- Reliability+yield study.
- Construct X-part demonstrator board, possibly with FPGAs.
- F-part preliminary design.
- F-to-X preliminary design.
- M&C preliminary design.
- CBF preliminary design.
- Total risk and cost analysis.

Summary

- Physical layout to try to minimize cabling…P2P F-X fiber.
- No monolithic corner-turner.
- Use existing and emerging technologies. ASIC for low power.
- Holistic approach—VBA. Possibly subsume some image processing in correlator.
- Phase-I: not good match…FPGA boards instead.
- Way forward.