



# The UniBoard

a RadioNet FP7 Joint Research Activity

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# Overview

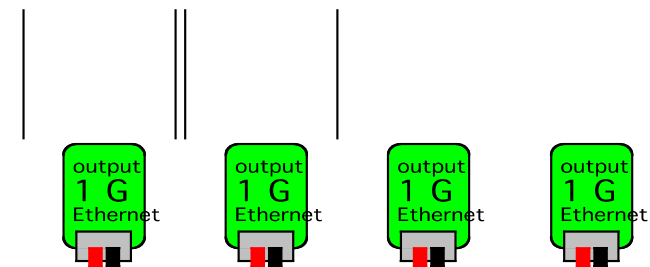


- Background, project setup
- Current state
- UniBoard as SKA phase 1 correlator/beam former
- Future: UniBoard<sup>2</sup>

# The aim



- Creation of a multi-purpose scalable high performance computing platform for radio astronomy
- Originally proposed by Sergei Pogrebenko in the late 90s, as a single-board all-station correlator, became basis of project in 2006
- Combine as much CPU and as much memory as possible on a “reasonably” sized board (Pogrebenko melt-down criterium)
- Use standard interfaces as much as possible
- Only digital, nothing analog...
- Develop several different applications in parallel over time, force design to be as generic as possible



- **UniBoard: a RadioNet FP7 Joint Research Activity**, 9 partners, kicked off January 2009
- **JIVE**: project lead, VLBI correlator
- **ASTRON**: hardware development, test firmware
- **INAF, University of Bordeaux**: digital receiver
- **University of Manchester**: pulsar binning machine
- **University of Orléans**: RFI mitigation algorithms
- **KASI**: VLBI correlator
- **ShAO**: digital receiver, VLBI correlator
- **University of Oxford**: all-dipole LOFAR correlator
- Strong support from collaboration, large amount of matching effort, financial contribution



# Supporting projects



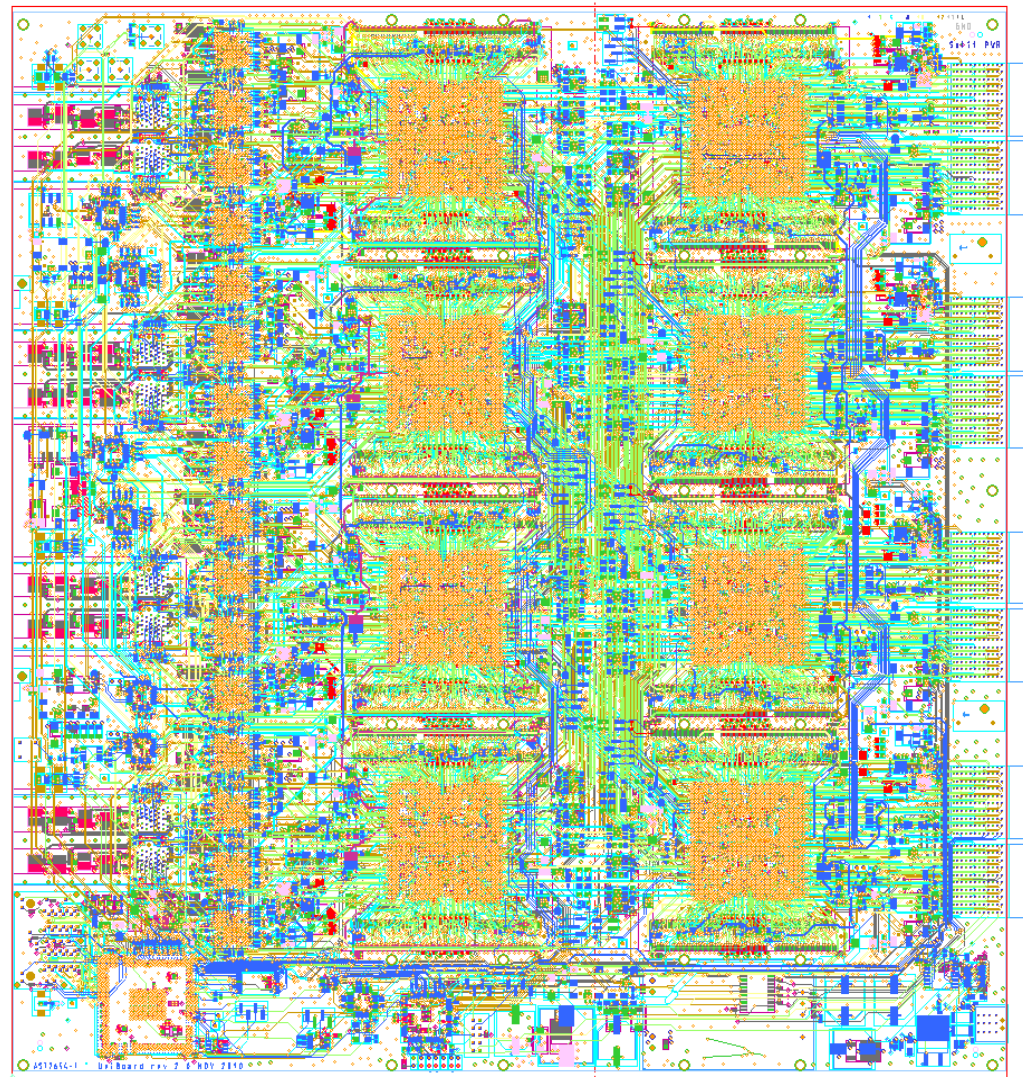
- ExBox: Expandable Box for X-correlation
  - JIVE/ASTRON proposal to NWO
- Build prototype FPGA EVN/APERTIF correlator
  - Using LOFAR expertise and technology
  - Backplane with several boards
  - Matching funds for UniBoard
- NWO - ShAO collaborative agreement
  - Stimulate collaboration between JIVE and ShAO in the development of FPGA-based correlators and VLBI space science applications
  - Several positions: students, postdoc, engineer



# The design



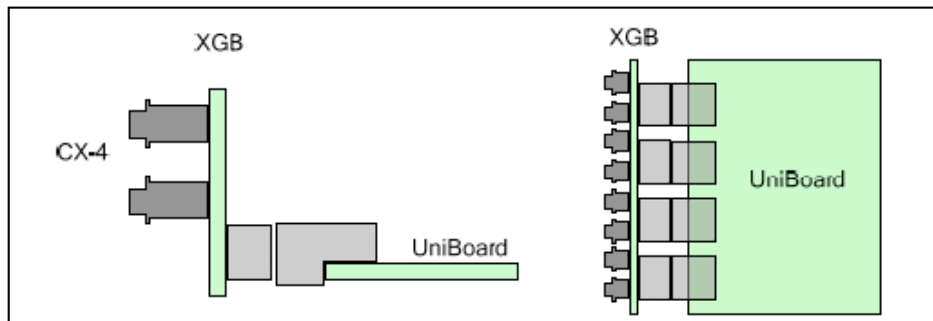
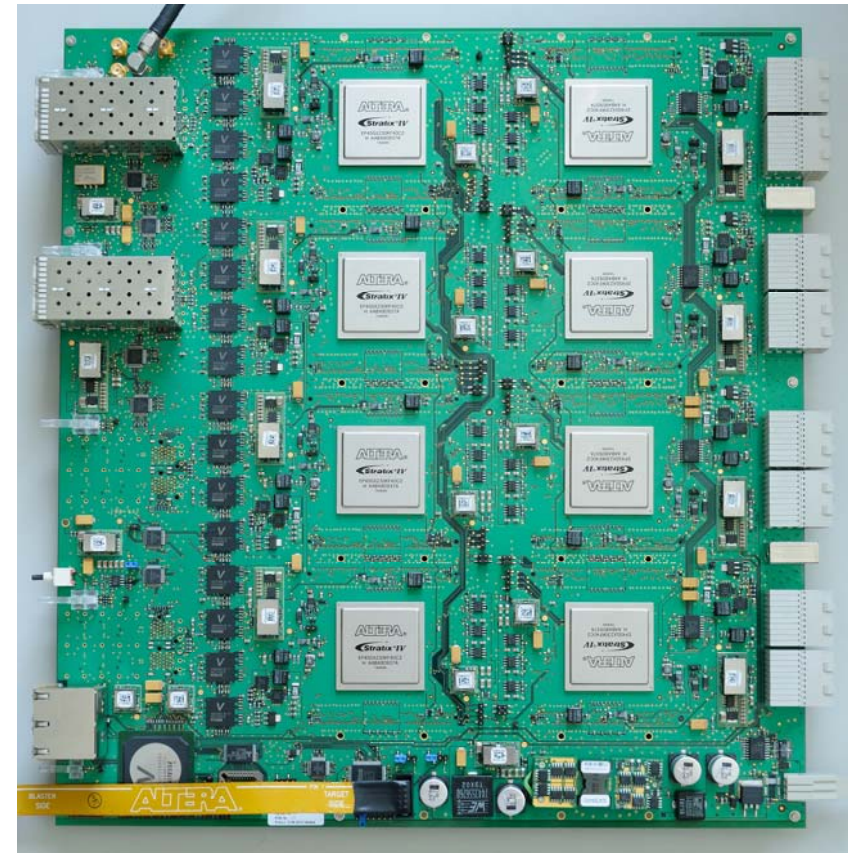
- 14 Layers
- 340x366mm
- 7304 components (47% of board space in use)
- 25798 connections
- 271 meter traces



# The result



- Per board: 8 Altera Stratix IV FPGAs (40 nm, 1288 18x18 multipliers, 400MHz, ~0.5TMAC/s)
- Per FPGA: 2 DDR3 memory banks (on backside of board)
- Four times four 10-GbE links connect to the front nodes via four SFP+ cages
- high speed mesh connects each front node to all back nodes
- The back nodes in their turn connect via four times four 8-bits LVDS to a backplane connector
- a 10G break-out board (the XGB) has been designed in the form of a mini-backplane, with a total of 16 CX4 connectors
- Prototype delivered May 2010, production run completed



Exploring the Universe with the world's largest radio telescope



# Applications under development



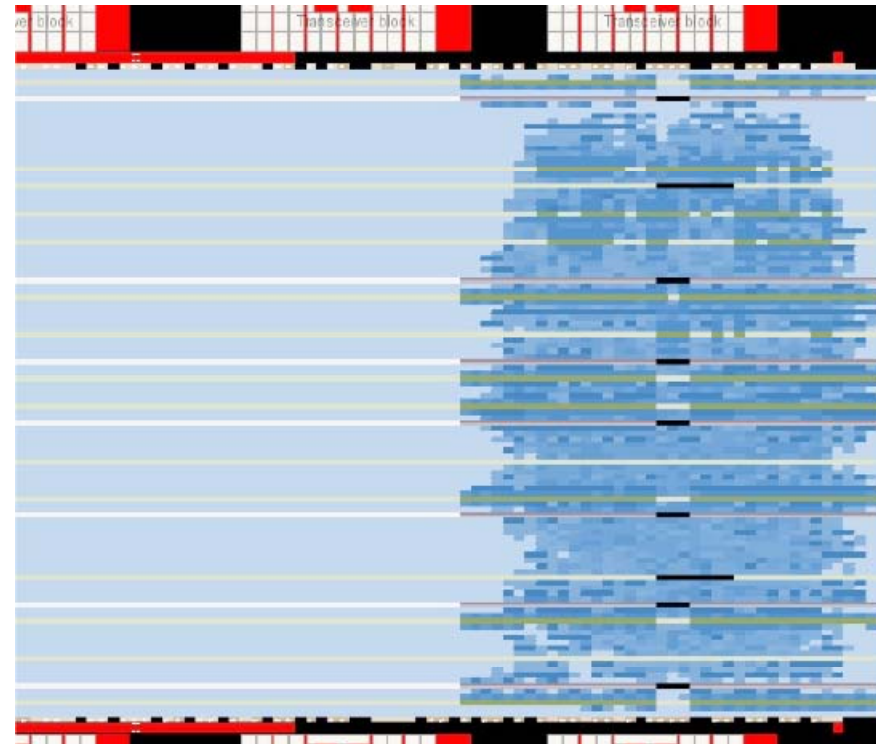
- **Currently under development:**
  - VLBI correlator (JIVE)
  - digital receiver (INAF, BORD)
  - pulsar binning machine (UMAN)
  - RFI mitigation (UORL)
- **Coming soon:**
  - APERTIF correlator (ASTRON)
  - APERTIF beam former (ASTRON)
  - AARTFAAC all-dipole LOFAR correlator (ASTRON + University of Amsterdam)
  - all-dipole LOFAR correlator (Oxford)
  - ShAO 65 meter telescope backend
  - Chinese/Korean VLBI correlators
  - more applications on the way



# Current effort in Dwingeloo



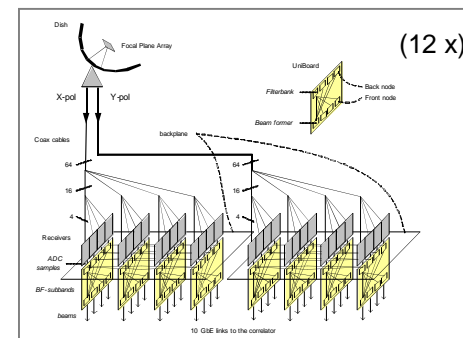
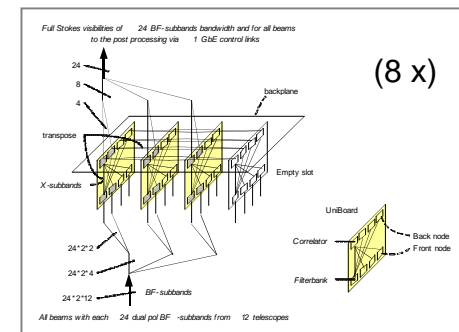
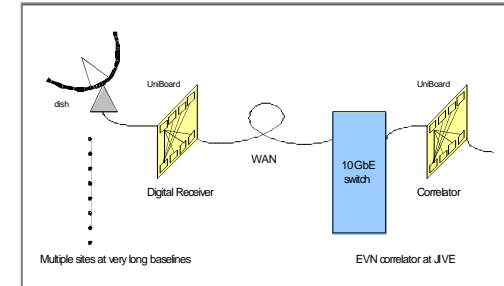
- Hardware design: Gijs Schoonderbeek, Sjouke Zwier
- Test firmware (+ testing): Eric Kooistra, Daniel van der Schuur, Jonathan Hargreaves
- Board control, correlator control system: Harro Verkouter, Des Small
  - Written in Erlang
- VLBI correlator firmware: Jonathan Hargreaves, Salvatore Pirruccio, Jintao Luo



# Different configurations



- **Combination of UniBoards into larger systems via backplane**
- Will be developed through NWO-funded ExBox project
- Application in APERTIF (ASTRON)
  - Correlator for 12 dual pol dishes, 300 MHz bandwidth, 37 beams
- Application in AARTFAAC (University of Amsterdam-ASTRON collaboration)
  - Correlator for 576 signal paths, ~ 17.5 MHz bandwidth

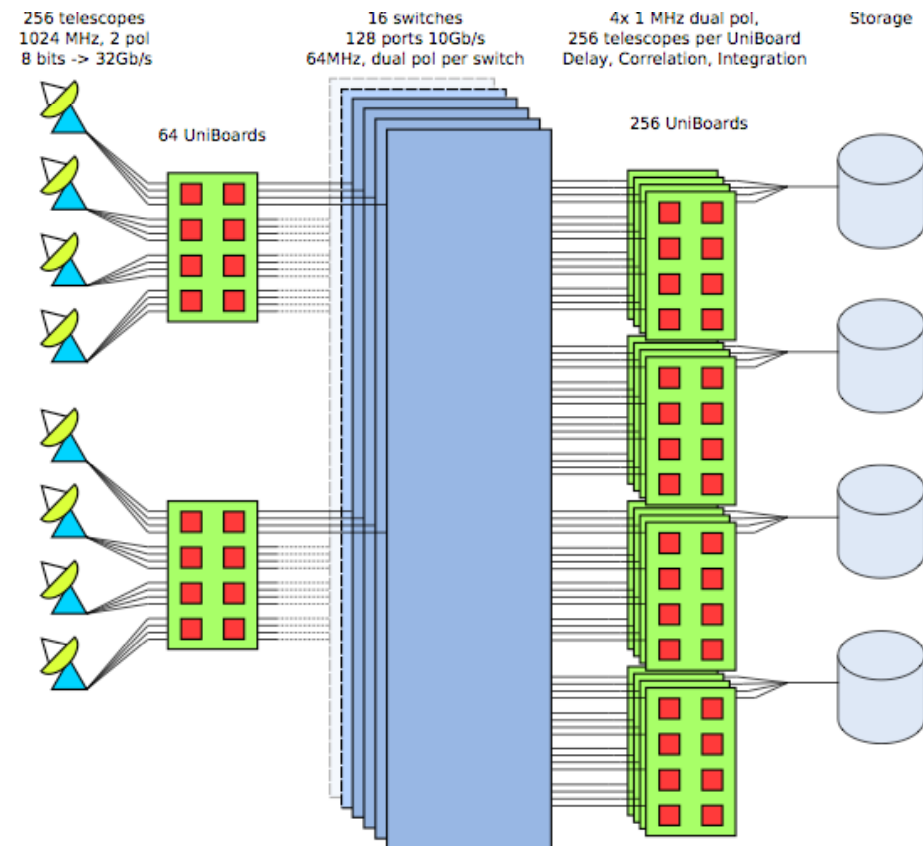


# SKA mid-frequency correlator (1)



## Mid-frequency:

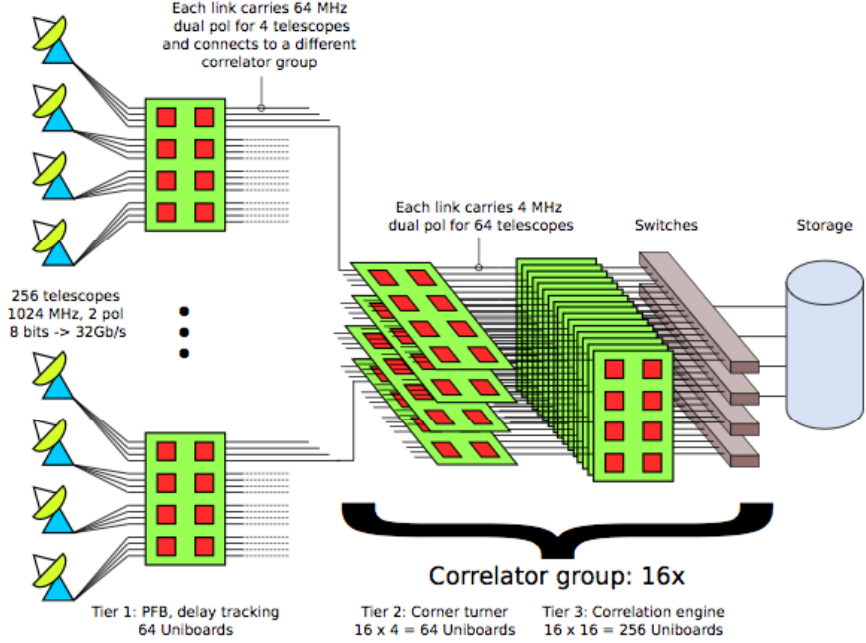
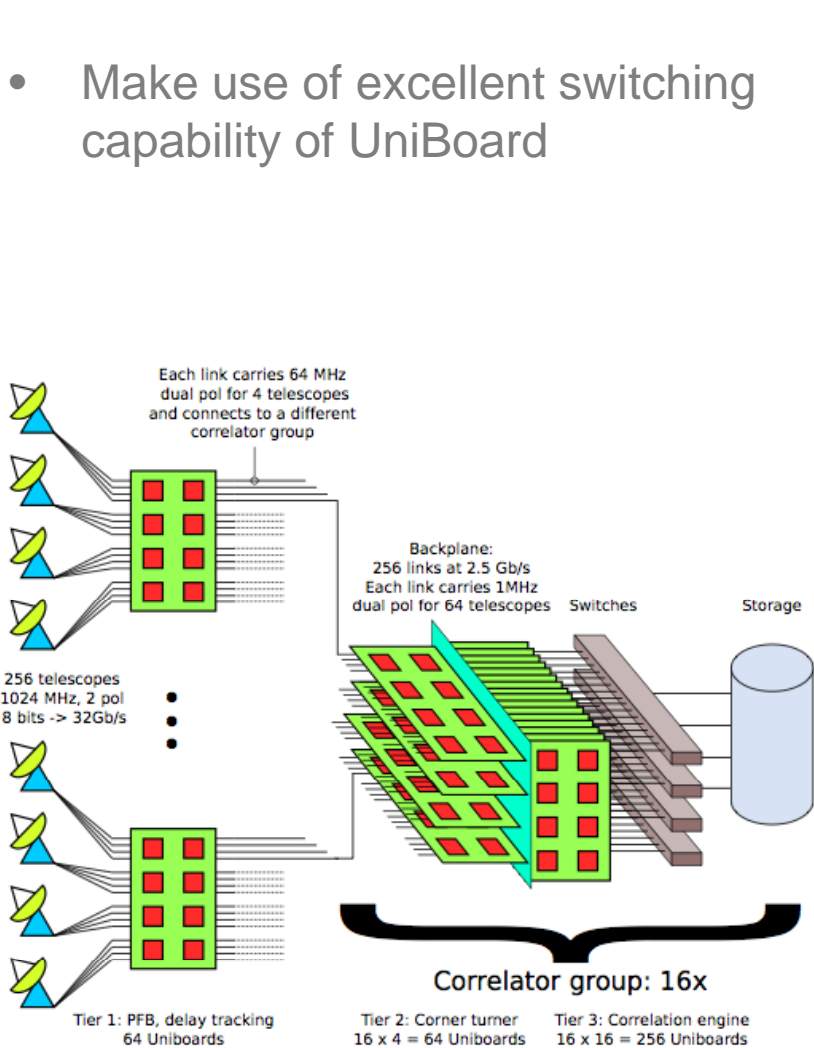
- 256 telescopes
- single pixel feeds
- 1024 MHz instantaneous bandwidth
- 2 pols
- 8 bits representation
- 7.5 kHz maximum resolution
- 0.1 s minimum dump time



# SKA mid-frequency correlator (2)

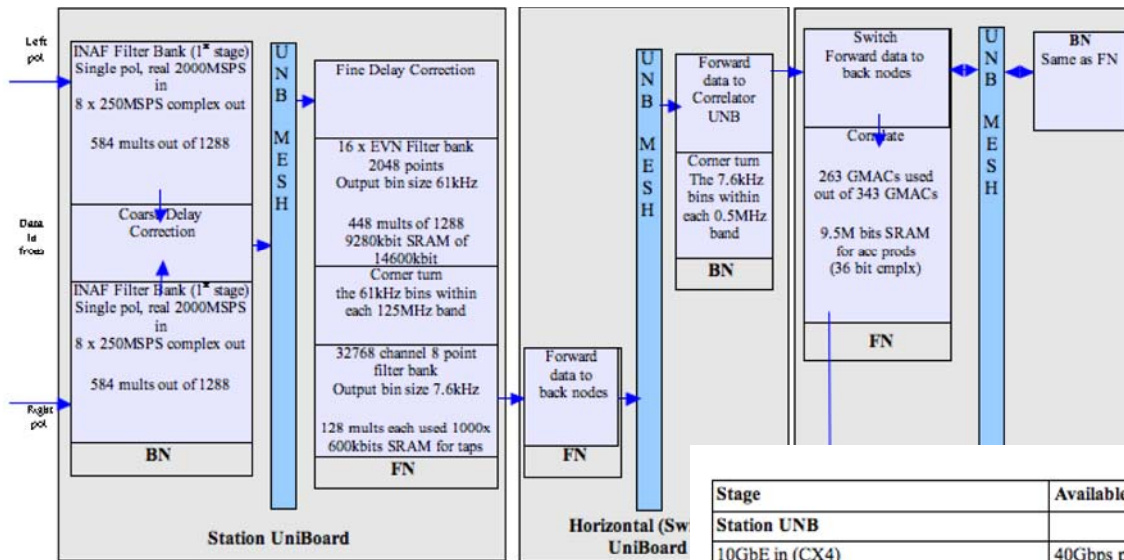


- Make use of excellent switching capability of UniBoard





# SKA mid-frequency correlator (3)



- 384 boards
- ~170 kW
- ~3.8 Meuro
- Feasible...

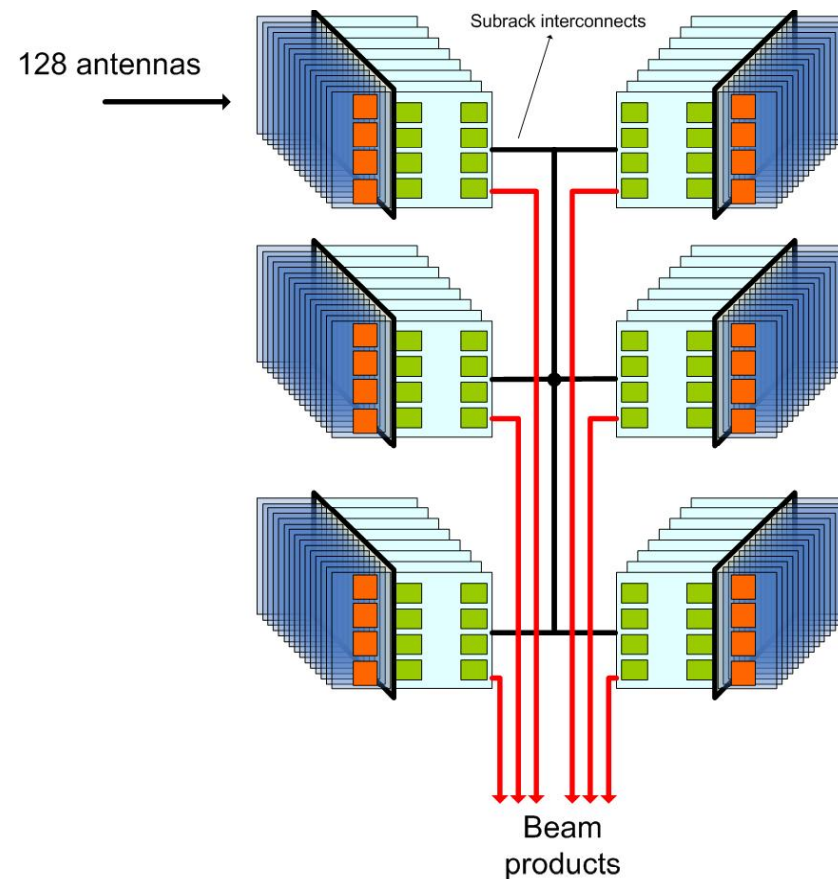
Stage	Available Bandwidth	Needed Bandwidth
<b>Station UNB</b>		
10GbE in (CX4)	40Gbps per BN 160Gbps per UNB	32Gbps per BN, 128Gbps per UNB
Or LVDS in	32 LVDS pairs per BN	32 bits @ 512MHz DDR per BN
DDR3 coarse delay (BN)	68Gbps per DDR3 module	32Gbps read and 32Gbps write for 8 bit data
Mesh (BN->FN)	26Gbps per BN-FN pair	8Gbps for 8 bit data, 18Gbps for 18 bit data
DDR3 corner turning (FN)	68Gbps per DDR3 module	32Gbps read and 32Gbps write for 8 bit data
10GbE out (SFP+)	160Gbps per UNB	128Gbps per UNB
<b>Horizontal (Switch) UNB</b>		
10GbE in (SFP+)	160Gbps per UNB	128Gbps per UNB
Mesh (FN->BN)	26Gbps per BN-FN pair	8Gbps for 8 bit data
DDR3 corner turning (FN)	68Gbps per DDR3 module	32Gbps read and 32Gbps write for 8 bit data
10GbE out (SFP+ .. ?)	160Gbps per UNB	147Gbps per UNB
<b>Vertical (Correlation) UNB</b>		
10GbE in (SFP+)	160Gbps per UNB	9.2Gbps per FN, 37Gbps per UNB
Mesh (FN->BN)	26Gbps per FN-BN pair	2.3Gbps (including data hopped back to the FNs)
Mesh(BN->FN)	26Gbps per BN-FN pair	Need 1.15Gbps (the hopped data)
10GbE product out	20Gbps per FPGA, 160Gbps per UNB	0.1s integration time, 7.6kHz freq bin, 32 bit complex output: 5.3Gbps per FPGA, 42.7Gbps per UNB 4.1s integration time, 7.6kHz freq bin, 32 bit complex output : 0.13Gbps per FPGA, 1.0Gbps per UNB

# SKA low-frequency beam former



## Low-frequency:

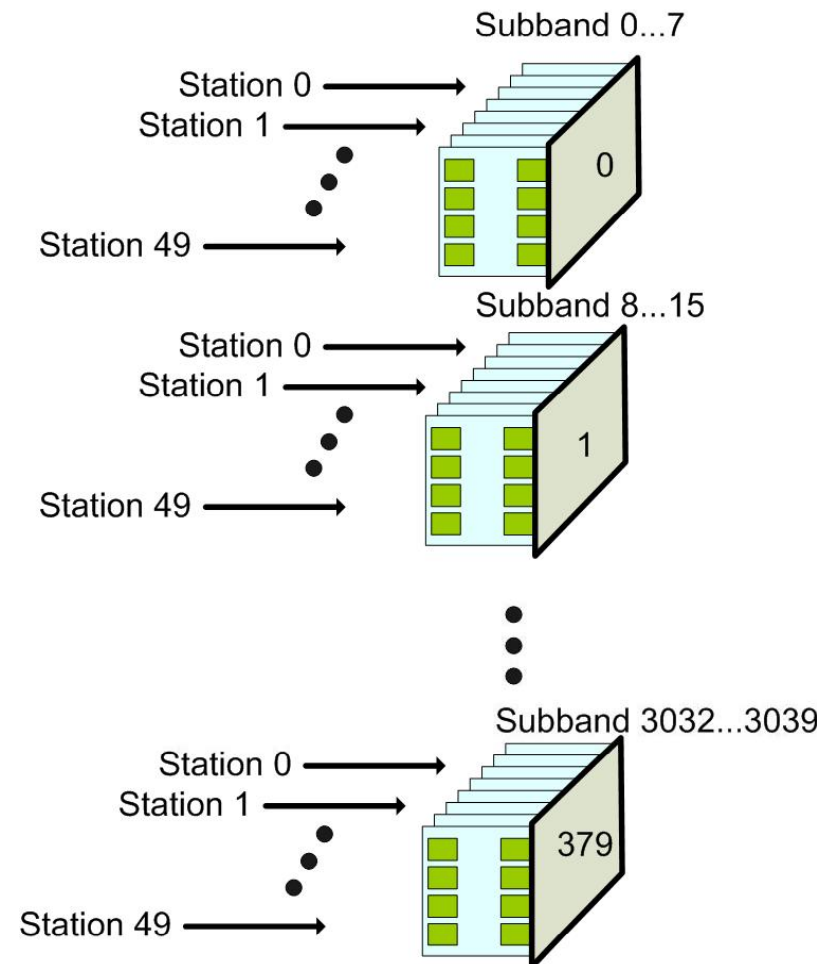
- Number of stations: 50
- Number of polarisations: 2
- Number of antennas / station: 11200
- Input bandwidth: 500 MHz
- Output bandwidth: 380 MHz
- Number of beams: 160
- Number of input bits from the station ADC: 8
- Number of output bits to the correlator: 4 x 2
- Subband width: 125 kHz
- Channel width: 1 kHz



# SKA low-frequency correlator



- 50 stations, 160 beams
- (correlation + beam forming)
- 9414 boards
- 90 Meuro
- 3.3 Mwatt
  
- But, *currently* available hardware
- ~2 generations of FPGA until 2015



# Next: UniBoard<sup>2</sup>



- Possible Joint Research Activity in RadioNet3, follow-up of current project, start date 2012 (if approved by EC) (looking good)
- Received strong support from RadioNet community
- Same basic idea, development of generic hardware complemented by a number of applications
- Consolidate and build on expertise obtained through UniBoard project
- **Strong emphasis on power efficiency (green computing)**
- Production-ready in 2015/2016
  
- **Complete re-design, using the next generation 28 nm FPGAs**, possibly one generation beyond that (some slack in start date of project)
- **Non-leaded components**
- Possible use of **40GE, 100GE**
- Investigation into effects of **hard-copy** and **partial hard-copy**
- **Tuning of algorithms and firmware design** to minimize power consumption
- **Balancing of system parameters and performance** to minimize power consumption
- **Standardized interfaces and coding conventions** to facilitate sharing and re-use of firmware blocks among developers of different applications