Phase 1 Correlator

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Background to the design

- CSIRO has been building high performance DSP boards for a number of years.
- Design philosophy evolving and continues to do so
- SPF correlator is an evolved version of Redback while the AA correlator requires a new approach

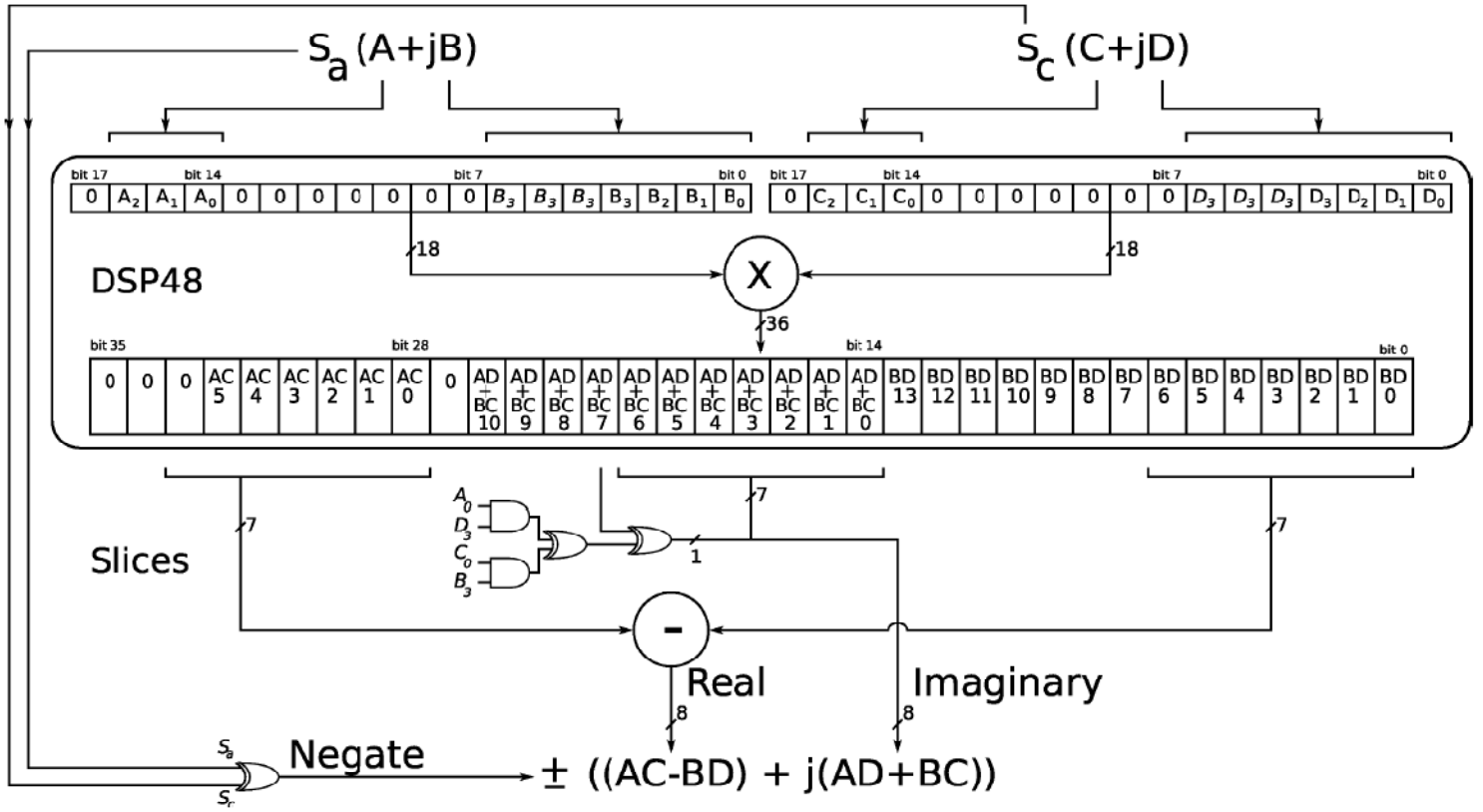
	Number Processing FPGAs	No 64 bit DRAMs interfaces	18bit Muliplie rs	Input data rate	Technology
MOPS	17	2	1496	20 Gb/s	Virtex II Pro
SKAMP	14	4	1680	40 Gb/s	Virtex 4
CABB	10	6	3056	40 Gb/s	Virtex 4 and II Pro
Redback1	4	4	2560	120 Gb/s	Virtex 5
Redback2	4	4	3072	160 Gb/s	Virtex 6

Phase 1 Correlator
Setting the scene FPGA

- Before attempting the design of the Phase 1 correlator we need to choose a technology – For this design FPGAs
- FPGAs 2011-12 devices have up to 4000 multipliers but mid sized devices (2000 multipliers) give better cost to performance
- Two more generation 2015-2017, it is estimated midsized devices have 8000 multipliers and 3.6T multiplication/s = 3.6TCMAC/s sec

4-bit Complex Multiplier In one 18 bit Real Multiplier

- Put “unsigned” 4 bit real and imaginary in top an bottom of 18 bits
- After multiply have real. Imaginary is sum top and bottom bits
- Adjust signs for final result
- Complex correlation per 18-bit multiplier, CMAC rate=Multiply rate



Further assumptions

- 10Gb/s optical are now becoming commodity items – Design will assume these are used for antenna-correlator links
  - 40Gb/s optical at low enough cost will lower cost and reduce amount of hardware to be built
- A shelf/card cage/chassis of boards can implement ~256 bi-directional optical link
- 8-bit ADCs and 4+4bit complex into correlator

Correlation Requirements

	Number of antennas	Processed Bandwidth GHz	Beams/ antenna	Correlation TCMAC/s	Min No. FPGAs
Sparse Aperture Array	**50**	**0.38**	**480**	**900**	**250**
Dish with SPF, 0.45-1 GHz	**250**	**0.55**	**1**	**69**	**19**
Dish with SPF, 1-2 GHz	**250**	**1.00**	**1**	**125**	**35**

- Number of FPGAs low compared to EVLA, ASKAP etc
- Data I/O will define correlator
- Additional requirement – tied-array beams

Aperture array data

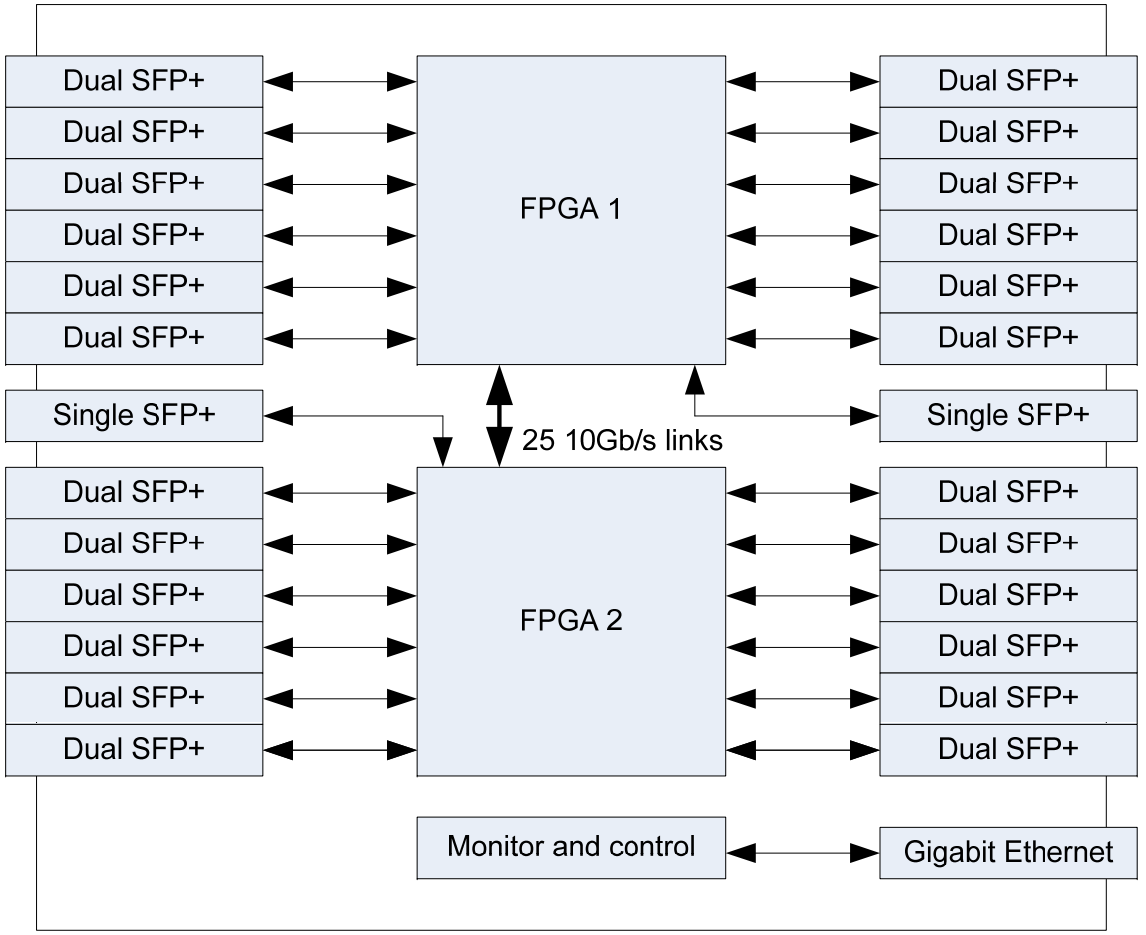
- Total bandwidth from AA
  - 380MHz x 480 beams x 2 polarisation
  - 365GHz
- ADC data at least 8 bit, filterbanks at high precision – suggest reduction to 4-bits for correlator in AA beamformer
  - Filterbanks part of AA station processing
- Data from station at frequency resolution and bit precision for correlator, minimise data transport
- Data is 8 bits/Hz = 2.9 Tb/s, for 10Gb/s links at least 290 fibres per station
- Not infeasible, ASKAP has 192 fibres per antenna.

Fibre Requirements

- Each 380MHz single pol beams generates 3.04Gb/s of data
  - Fit 1.5 dual pol. beam on single 10Gb/s fibre
  - Half beam is 190MHz dual polarisation
  - 320 fibres per AA station
- Min correlation module process a single fibre from each of the 50 stations.
  - “Pizza” box sized module with
  - Single board
  - 50 input fibres
  - Power supplies, cooling and command and control

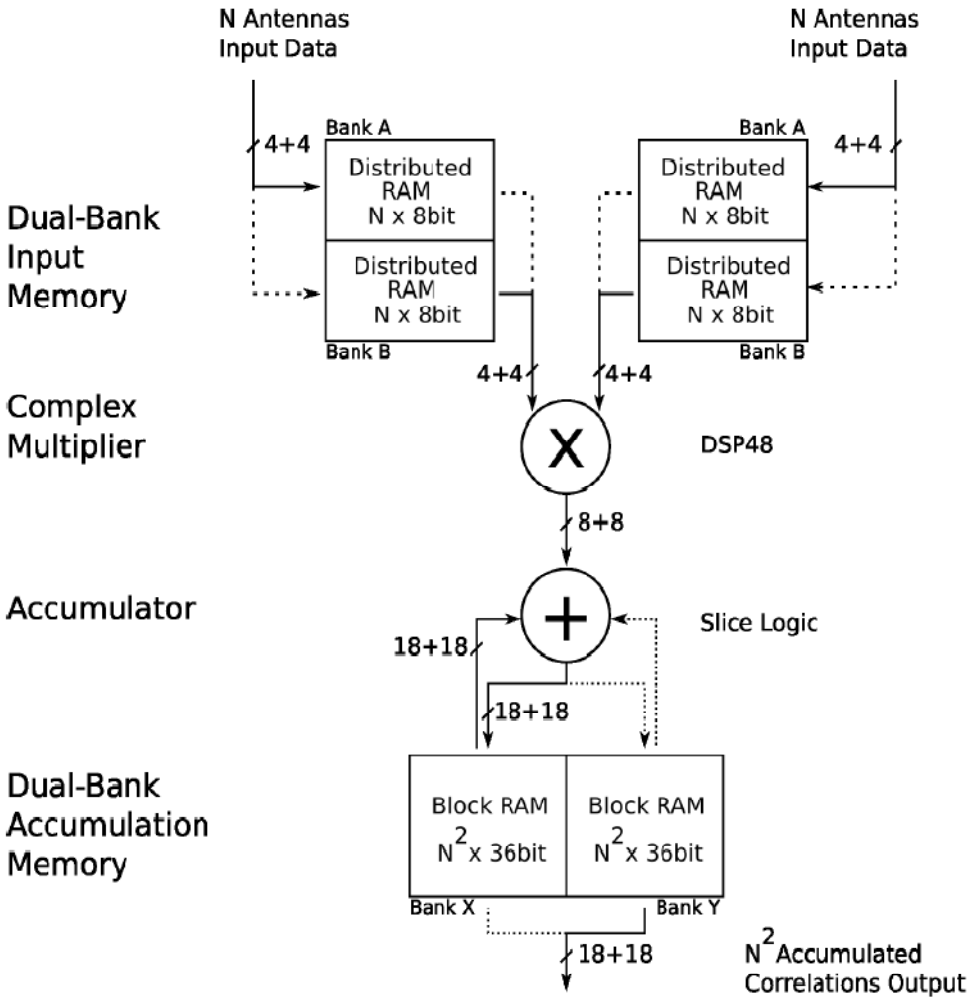
“Pizza” box correlator board

- 25 dual height SFP+
- Two FPGA design shown
- Very simple to build (layout time weeks)
- FPGAs with required I/O already exist



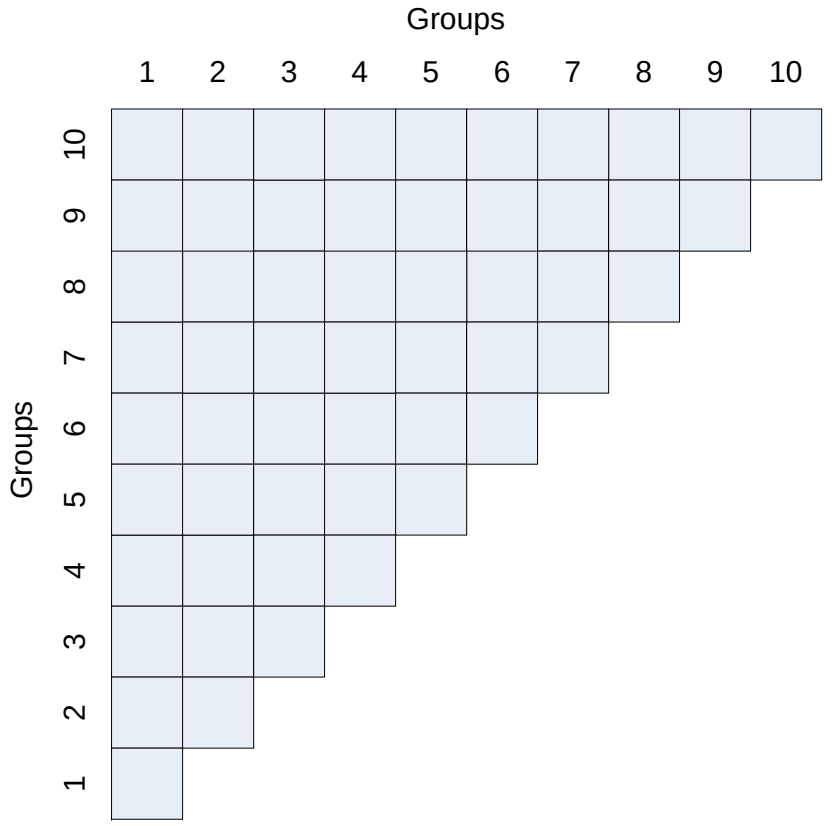
Correlation Cell

- Two sets of N inputs correlated
- N^2 correlations
- N=10, clock=450MHz
  - Process 4.5MHz BW
  - Any number of channels within BW
    - 1kHz channels, each cell process 4500



All baselines at one time

- AA correlator 50 dual pol. inputs
  - 10 groups of 10
- 55 correlation cells to form all baselines/Stokes
- 45 cells unlike groups
- 10 cells same two inputs
  - Some duplication
  - Autocorrelations
- 4.5MHz for one beam processed with 55 multipliers



Processing for 1.5 beams

- Total bandwidth 380 x1.5= 570 MHz
- 4.5MHz for 55 correlation cells
  - 127 sets of 55 cells = 6,985 cells to process 570MHz
  - Single 2015-2017 midsized FPGA sufficient
- At AA station must send data for 127 frequency channels for ~1000 time samples on each fibre
- Arrange this as 127x1000 beam1 twice, followed by a set from beam 2, then repeat

Correlator output

- Proposed frequency resolution 1kHz
- Integration time 1.2s, integrate 1200 samples
  - Integrate within cell then dump no long term accumulator
- 50 AA stations = 5k correlation per 1kHz channel
- 570,000 channels = 2.85G correlation/s
- 64bits/correlation = 182Gb/s per “Pizza” box
  - 19 out of 50 SFP+ modules needed to dump correlations
  - High data output due to fine frequency resolution across wide bandwidth

Tied-Array beams

- Three types
  - Incoherent, sum power for corresponding beams
    - Sensitivity 7 times single station, Field of View is that of station beam, one single beam possible
    - Simple to produce – not considered further
  - Coherent, Phase up beams and sum
    - Sensitivity 50 times single station, small Field of View
  - Coherent sub-arrays, coherent beamforming for geographically compact sub-array, then incoherent beamforming
    - 5 groups of 10 then sensitivity 22 times single station
    - Much larger field of view than coherent
    - Exact analysis still to be done

Coherent Tied-Array Processing

- All data into correlator time aligned
- Beamforming simply complex multiply and add
- Use same 4 bit complex multiplier as correlator
- 1 multiply per input sample per TA beam
- Correlator 50 multiplies per input sample
- 50 TA beams same processing load as correlator
- But 480 station beams each with 50 beams
  - Total of 24,000 coherent beams possible by doubling FPGA resources (design shown earlier suitable)
  - IF coherent subarrays processing the same

Coherent Beam Output

- If coherent beam is still 4+4bit complex data then output of data has same data rate is input from one station
- SFP+ modules are bi-directional – up to 19 outputs (19 station input) used for correlator data
  - Leaves the equivalent of 31 station outputs
  - But some outputs have half the bandwidth, output available for average 25 coherent beams per station beam
  - 12,000 coherent beams in total for the cost of adding second FPGA to “Pizza” board
- Data in 1kHz bands process with synthesis filterbank
  - May need to oversample input data to eliminate aliasing

Coherent sub-arrays

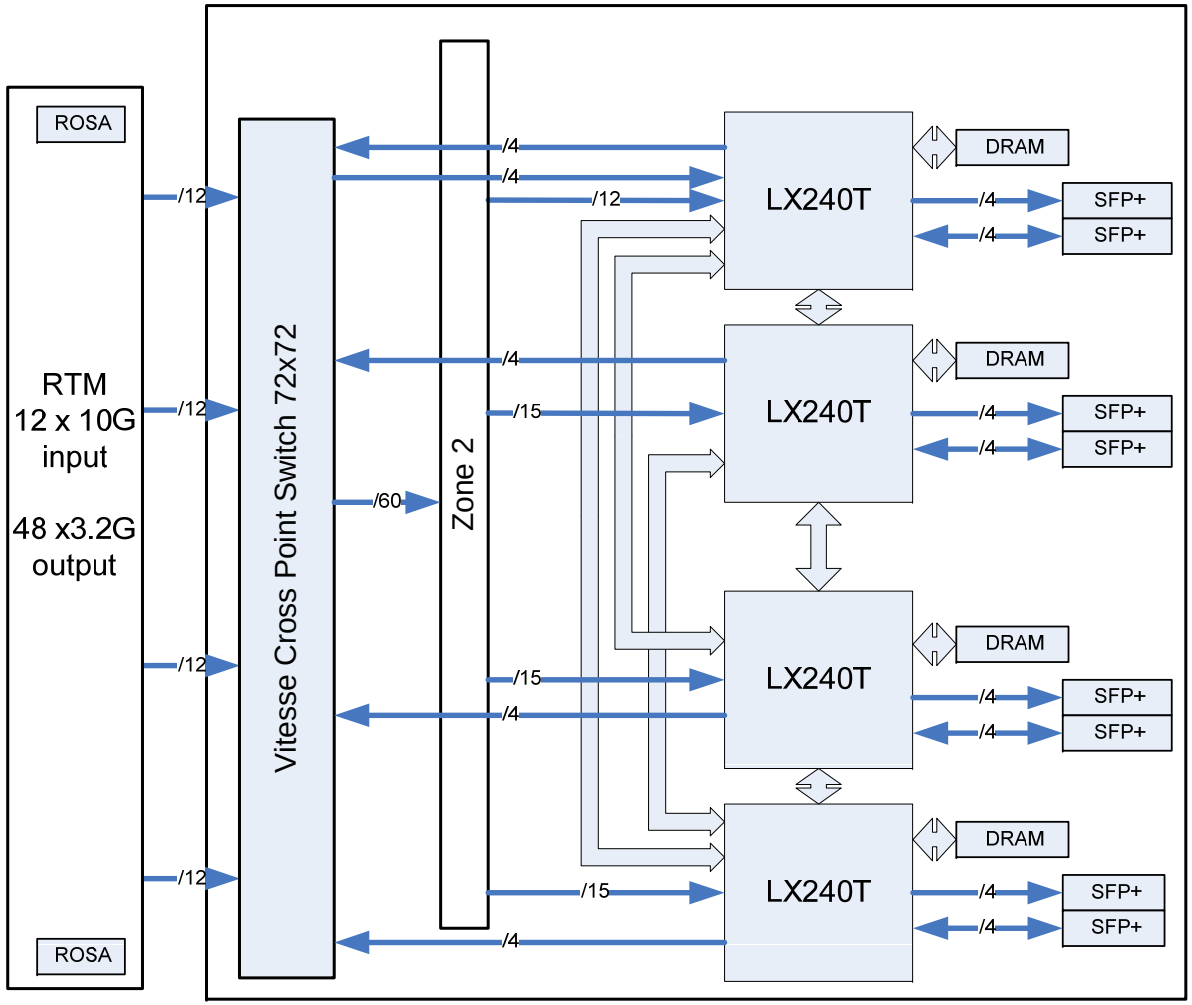
- Coherent within sub-arrays, incoherent between subarrays.
- After coherent beamforming want ~1MHz averaging , must average across frequency channels, also average across the two polarisations
- Arrange for 8 set of 127 contiguous frequency channels to be sent to correlator. Form average across all data ~1MHz
  - Gives 1200 1ms time averages per beam
  - 50 beams needs ~50 RAMs out of 8000, Storage not a problem
- One value for each 2000 inputs, 16kbits input results in 32bits output, 500:1 data compression.
- All data output on single 10Gb output.
- Can achieve full 50 beams/station beam = 24,000 beams

Single Pixel Feed Correlator

- "Pizza" box has 50 inputs – not suitable for 250 dish SPF correlator – new design
- Single shelf can take a single 10 Gb/s fibre from each dish.
  - 16 boards per shelf
  - 16 inputs per board (Redback2 has 16 already)
- Standard AdvanceTCA shelf, COTS back plane has 4 high speed links from a board to each slot
  - Including data kept on board this is 64 links
  - Links need only run at 2.5Gb/s to implement a full cross connect of all input data (6Gb/s available if needed on COTS backplane)
- Much of processing common with AA
  - Filterbank/data reordering at antenna, correlation cell, tied array processing

Redback2

- Meets Phase 1 input requirement
- All links 3.2G or LVDS
- For Phase 1
  - direct 10G input to FPGA, removes cross point switch
  - All internal link 3.2G sufficient,
  - no LVDS simplifies design



Antenna electronics

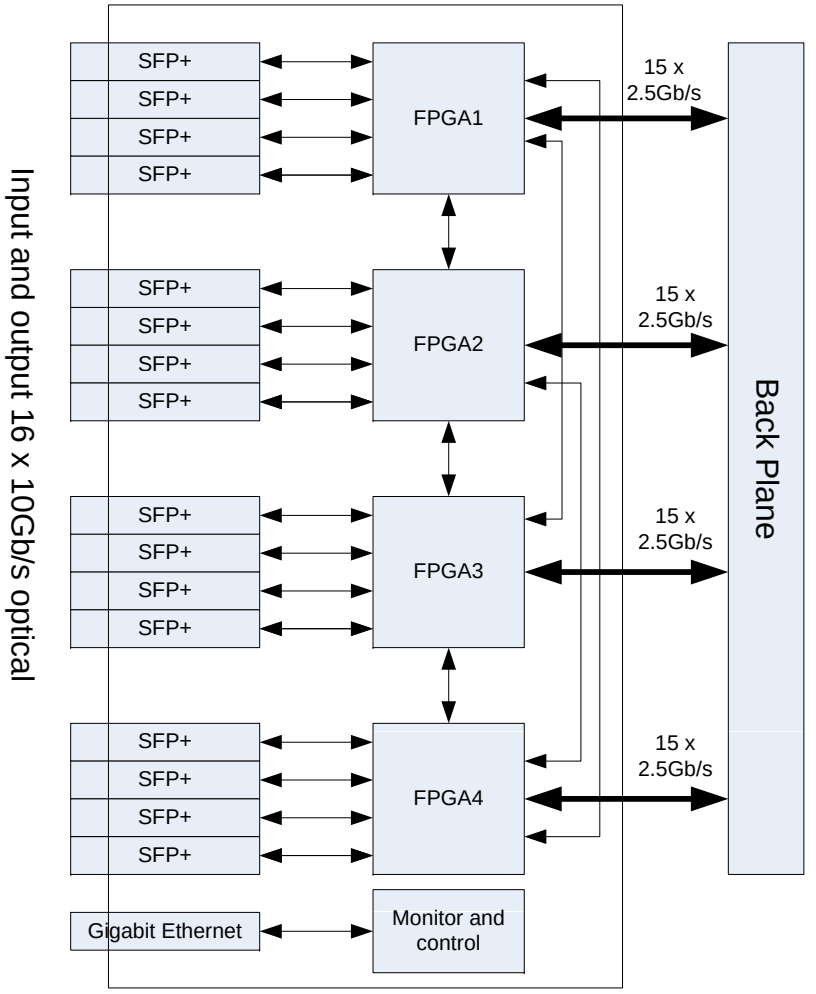
- ADC, filterbank and optical transmitters at antenna
- Example, ASKAP DragonFly, Two ADCs, FPGA and 4 SFP+ modules
  - 4x300MHz or 2x600MHz
  - Upgrade FPGA, 2x5Gs/s ADC and add DRAM for Phase1
- DRAM for data reordering
- Output 2 x 1GHz x 8bit/Hz
  - 16Gb/s
  - Two 10Gb/s optical sufficient

SPF Phase 1 correlator

- Two 10G optical outputs per antenna
  - Two AdvancedTCA shelves
- 35 FPGAs for correlation, same for tied-array
  - 32 boards in two shelves = 3 FPGAs per board
- Use same correlation cell but 16 inputs/group, 256 correlation/cell = 488 cells for all baselines
  - Can do 16 frequency channels per FPGA at one time
- Frequency resolution 10kHz over 1GHz
  - $2x250^2$ correlation x 10^5 channels x 64bit/correlation
  - 25Gb/s per board correlator output
  - Leaves 10G outputs sufficient for ~200 coherent beams

Possible board design

- Four smaller FPGA with 4x10G direct connect
- 4 quad SFP+ on front panel
- Inter-FPGA links 5Gb/s
- Backplane 2.5Gb 8b10B encoded
- ASKAP low overhead monitor and control
- ~100 data lines to route
- Relatively simple board
  - Layout weeks not months
- No need for RTM
  - Reduces cost



PAF and WBSPF correlator

- For a Phased Array Feed (PAF on a dish) the correlator consists of reproductions of SPF correlator shelve
  - cost is just proportional to the total bandwidth
- For Wideband Single Pixel Feed increased BW
  - 1-10GHz
  - 9 times the bandwidth of 1GHz BW SPF
- PAF probably octave bandwidth - 500MHz
  - Large PAF has 36 beams
  - 18 times the bandwidth of 1GHz BW SPF correlator
- Does not include cost of PAF beamformer
  - Previous presentation

Estimated cost

- Can construct in 2014 or 2017
  - Two successive FPGA generation
  - Cost includes FPGA capacity for coherent tied-array beams
  - Higher cost in 2014 due to extra FPGAs

	2017 Cost	2014 Cost
AA	2.2M€	2.6M€
SPF	0.16M€	0.2M€
WSPF	1.4M€	1.8M€
PAF	2.8M€	3.7M€

Cost saving

- If not many coherent beams are needed then many optical outputs unused
- Replace SFP+ with ROSA (Receive only modules) save ~60€ each transmitter removed
- Save 20k€ SPF, 200k € WBSPF, 400k€ PAF, 500k€ AA
- AA, SPF, WBSPF and PAF correlator ~ 4M€ 2017

NRE

- Correlator firmware simple and will have been developed for previous project. Low overheads for correlation and tied array beamform
- Data transport firmware negligible in AA and comparatively simple in SPF
- Total firmware effort ~2 man years
- Hardware simple total for both design less than 1 man year, prototype and production designs
  - Prototype runs low cost
- Some effort may be needed for “Pizza” box mechanical and cooling,
  - Borrow Roach design?

Conclusion

- Hardware designs for AA and SPF correlator
  - Simple easy to implement boards
- Firmware simple
  - Total hardware and software NRE less than 1M€
- Hardware cost less than 2.4M€ for SPF and AA
- PAF correlator adds 2.6M€
- High cost for optical inputs, 1M€ savings if mostly receive only
- Extra 1.5M€ for full system in 2014