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Station Beamforming

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Station Beamforming

- …in principle covers AA low, AA mid and dishes. But –
- AA-mid now pushed back in to Advanced Instrumentation Programme. This is a *good* thing:
  - 'Difficulty' of a dense aperture array scales as at least ν^3_{max}
  - More new science with a 10% system in low band
  - Do the easy thing first and work up…
- Dish station beamforming only relevant to SKA-2
  - 200-input correlator is tractable
  - 2000+ correlator may not be…or may be.
  - If you do need it, it is trivial compared to the AAs: one dish station beamformer = one AA tile beamformer × a few
- **Focus on AA low**

Context and meta-questions

We have an 'official' spec (Memo 125) but –

- Very top level – many important questions unanswered
- Does it have full buy-in from the science side yet? 50 MHz?

Science requirements   System specs   Implementation

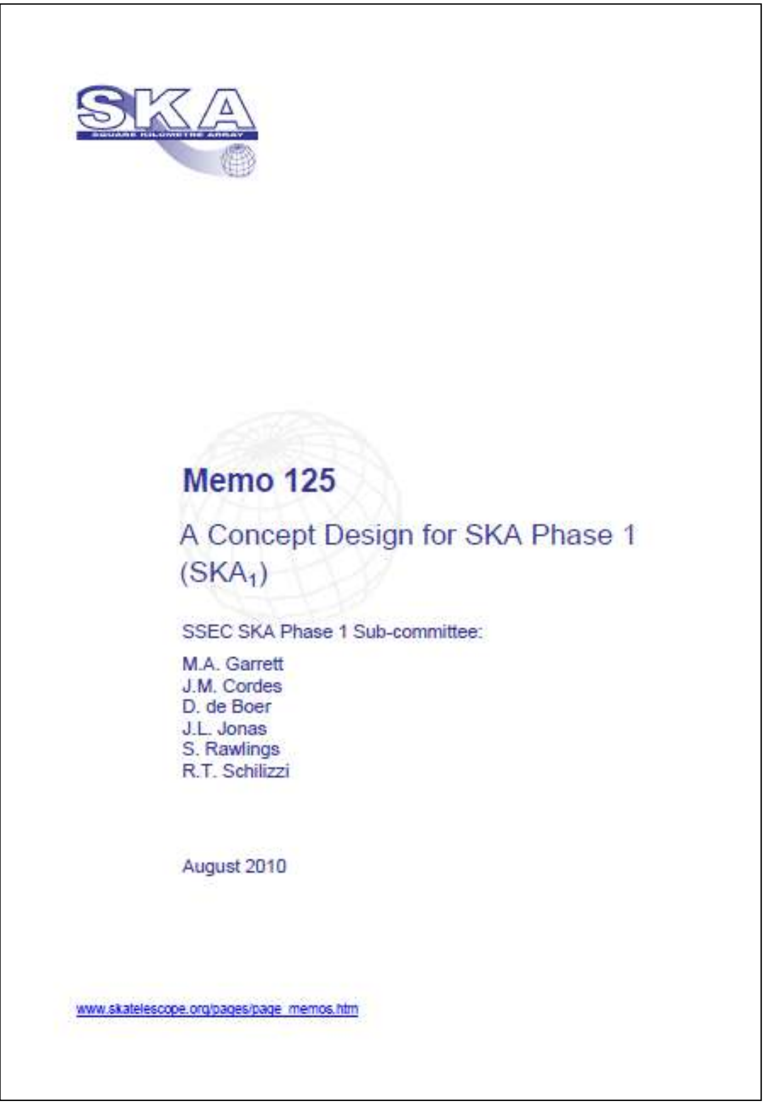
Both these loops need to be closed and iterated on!

What is the relationship between SKA-1 and SKA-2 requirements?

- Treat SKA-1 as 'stand-alone' instrument and optimise for that?
- Treat SKA-1 as prototype for SKA-2 and optimise for that?

During the SKA_1 design process, components of receptors used in SKA_1 that are difficult or impossible to change will be designed and reviewed against the requirements of the full SKA (i.e. they will be SKA_2 compliant). In some, hopefully limited cases, it will be necessary for SKA_1 sub-systems to be replaced in order to be compatible with SKA_2. Certain aspects, such as the

The spec as it stands…



Memo 125

A Concept Design for SKA Phase 1 (SKA_1)

SSEC SKA Phase 1 Sub-committee:

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www.skatelescope.org/pages/page_memos.htm

AA low:

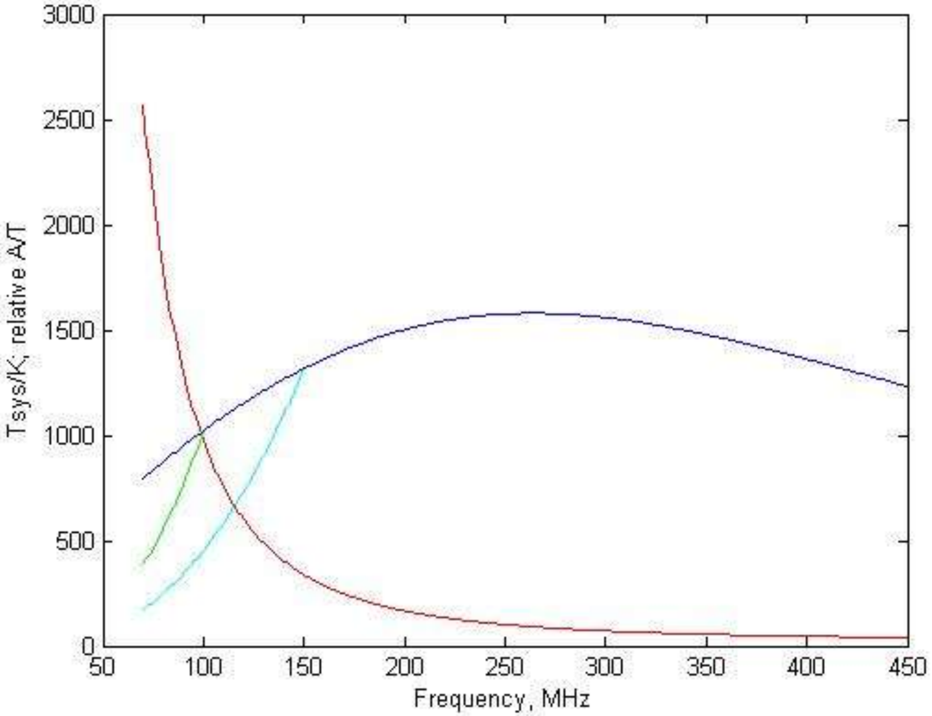
- Frequency 70 – 450 MHz (all available instantaneously)
- A/T ‘up to’ 2000 m^2/K
- Baselines up to 100 km

TBD:

- Number of stations
- Size of station (physical/number of antennas)
- Layout of stations
- Survey speed ie sky coverage

Points to note…

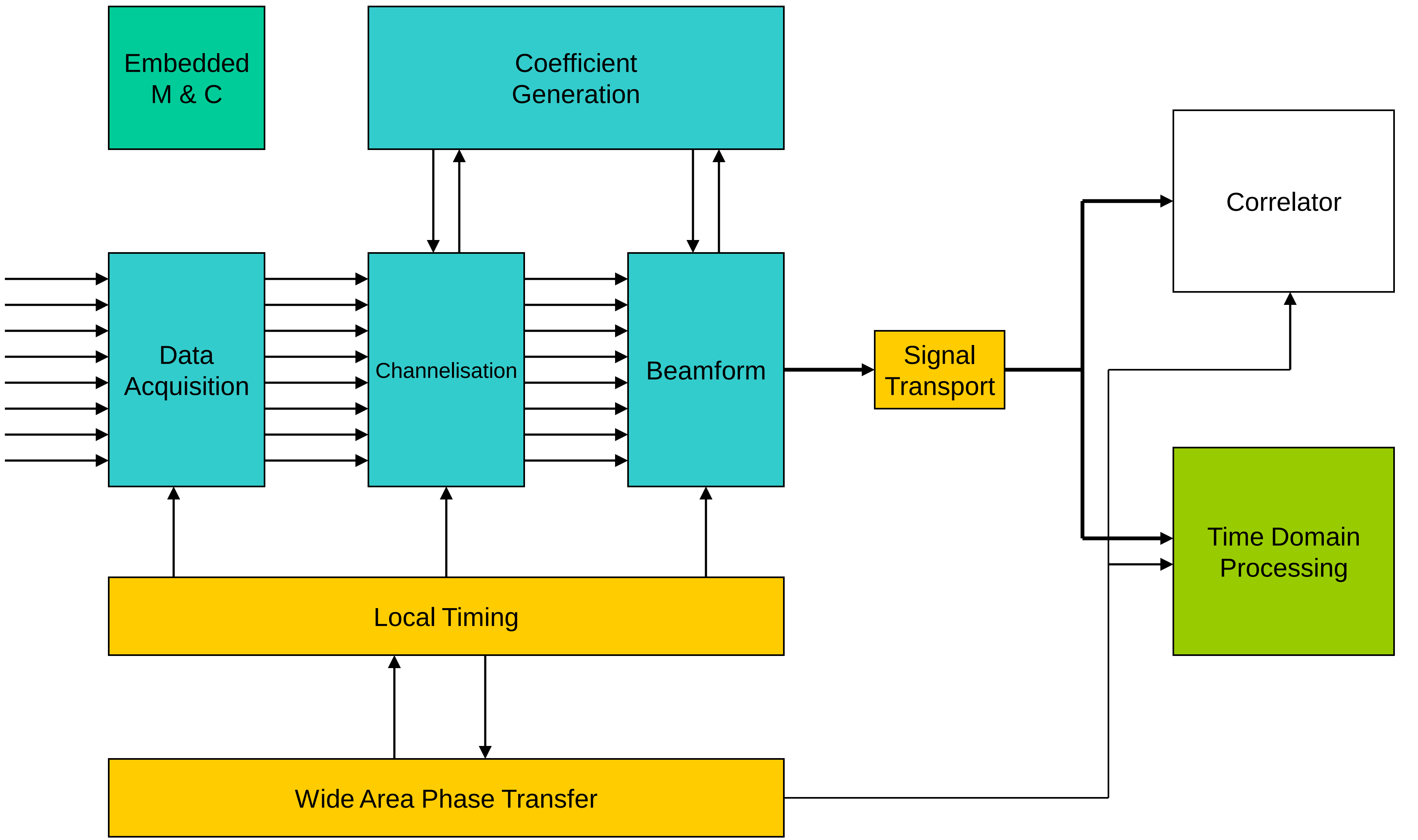
- 70 – 450 MHz is *huge*. The array is *very* sparse
- 450/70 = 6.4 = 2.7 octaves
- $(450/70)^2$ = 41. At the top of the band the array is 2.5% filled
- Critical spacing frequency? May be >70 MHz…but then lose A/T



Interfaces to rest of system

- Antenna → RF chain → Station beamformer → Data transport → Correlator
- Antenna/RF chain is important and not yet clear what solution is…but interface is clear
- Need to determine whether bottleneck in system is station processing, data transport or correlator…data transport?
- However these numbers still not clear…a very important overall spec driver. Station beamformers/data transporters/correlators need to talk very closely

The Digital System



The numbers game

- Bandwidth 70 – 450 MHz
- Instantaneous Bandwidth 380 MHz
- ADC Sampling at 1 GSa/s @ 8-bit
- Antenna Aeff = $\lambda^2/4$
- A/T of SKA Phase 1: 2,000m^2/K (at what frequency?)
  - T_{sys} = 1000K @ 100MHz; A_{eff} = 2,000,000m^2 = 3.5 million antennas
  - T_{sys} = 100K @ 250MHz; A_{eff} = 200,000m^2 = 550,000 antennas
  - T_{sys} = 50K @ 450 MHz; A_{eff} = 100,000m^2 = 900,000 antennas
- Let's take 1 million antennas as an estimate…
- SKA-2 (20,000 m^2/K) is 250 stations of 40,000 antennas each
- SKA-1 could be
  - 250 stations of 4,000 antennas
  - 25 stations of 40,000 antennas
  - Something in between…say 100 stations of 10,000 antennas

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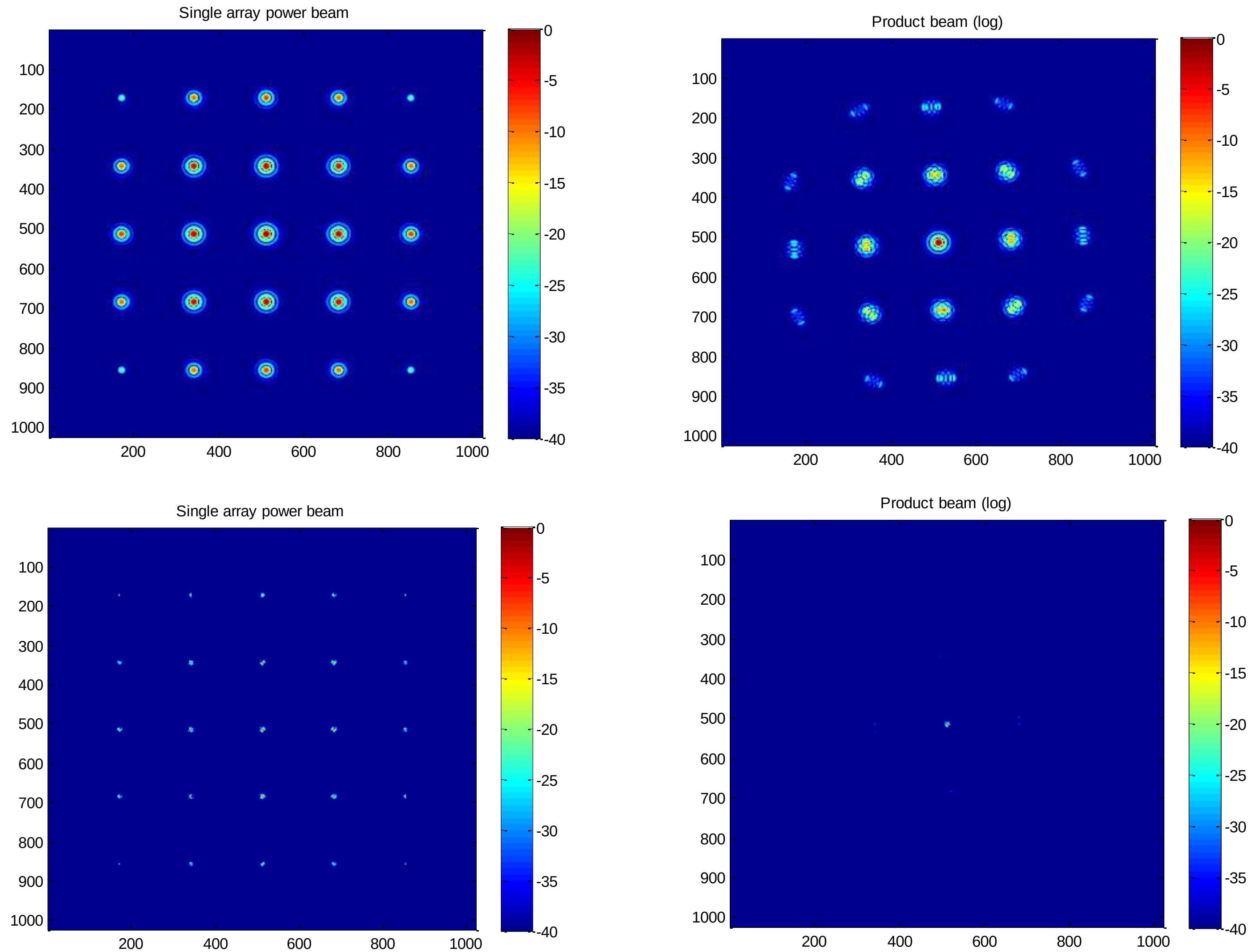
Station beams



- Array thinned by factor 6
- (top) radius 64 element positions
- (bottom) radius 256 element positions
- (L) power beam
- (R) cross beam rotated 6 deg

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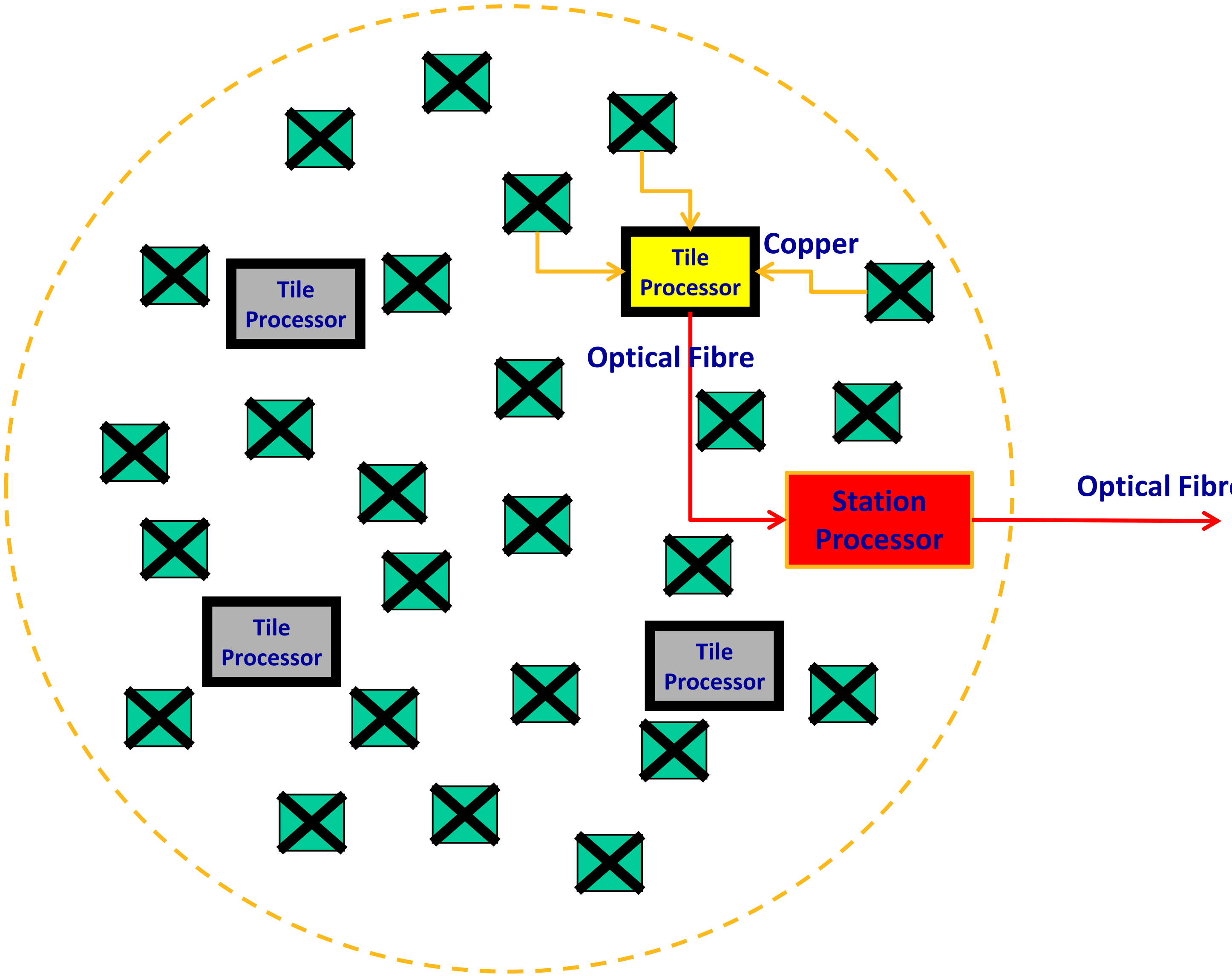
Numbers cont...

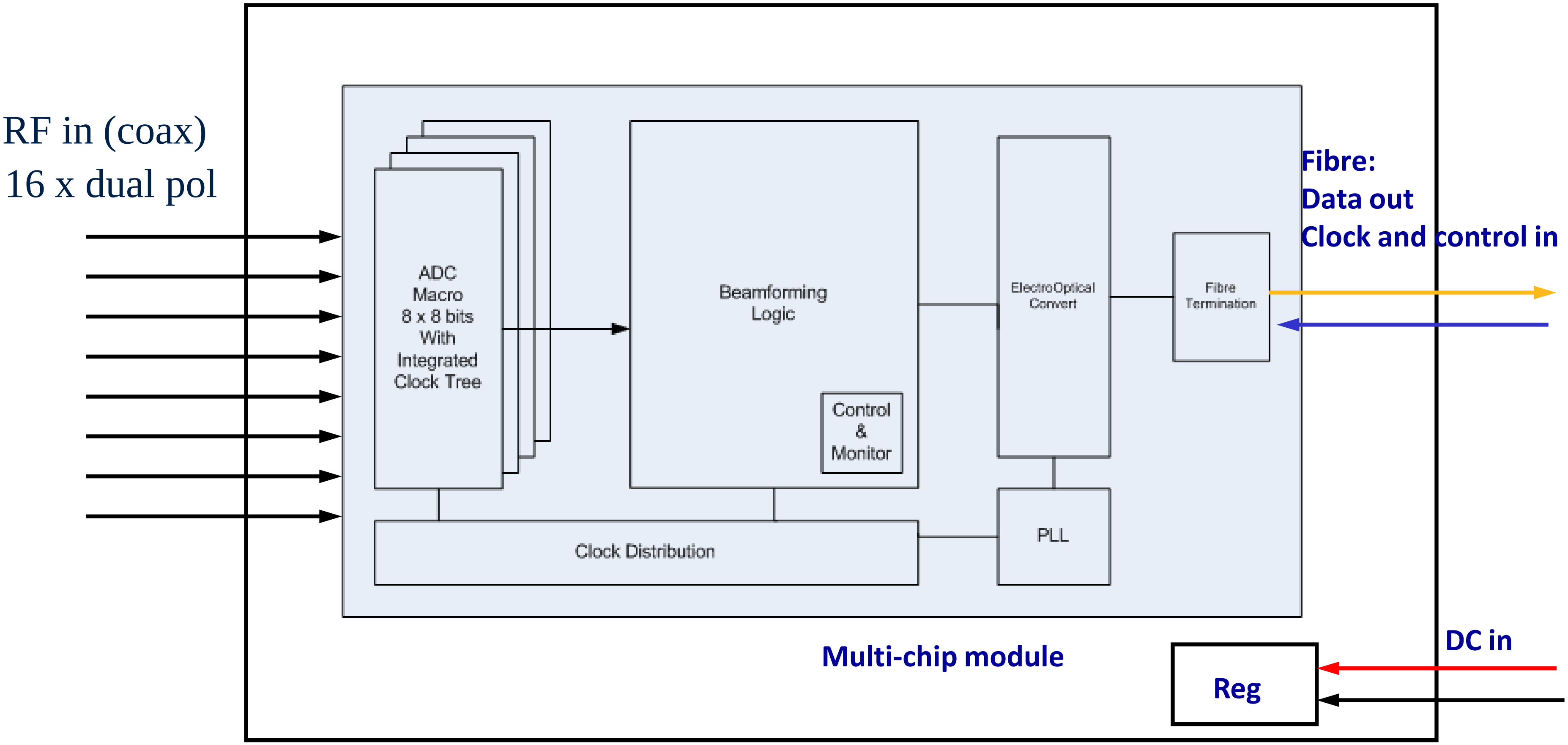
- SKA-1 ~ 100 stations of 10,000 antennas each
- Assuming λ/2 @ 70 MHz…
- Station diameter ≈ 240m
- Station beam @ 70 MHz ≈ 1°, @ 450 MHz ≈ 0.15°

- Nbaselines = 50,000
- Maximum fully filled aperture plane = 26 km
- == 33 arcsec @ 70 MHz, 5 arcsec @ 450 MHz
- Input data rate to station 160 Tb/s
- Output rate? Assert 1 Pb/s to correlator = 10 Tb/s off station = 100 x 100Gb/s fibres
- Output beams 2+2 bits, 100kHz channels = 12.5 million beam-channels – by DFT need 20 Pop/s
- Equalise sky coverage so N(f) ~f^2 – 100 beams in lowest (70 – 70.1 MHz) channel = 100 sq deg instantaneous coverage.
- Correlator has to do 50,000 baselines for each 100 kHz beam-channel ~ 100 Pop/s

Station Layout



Tile processor box



Space-Frequency Beamforming

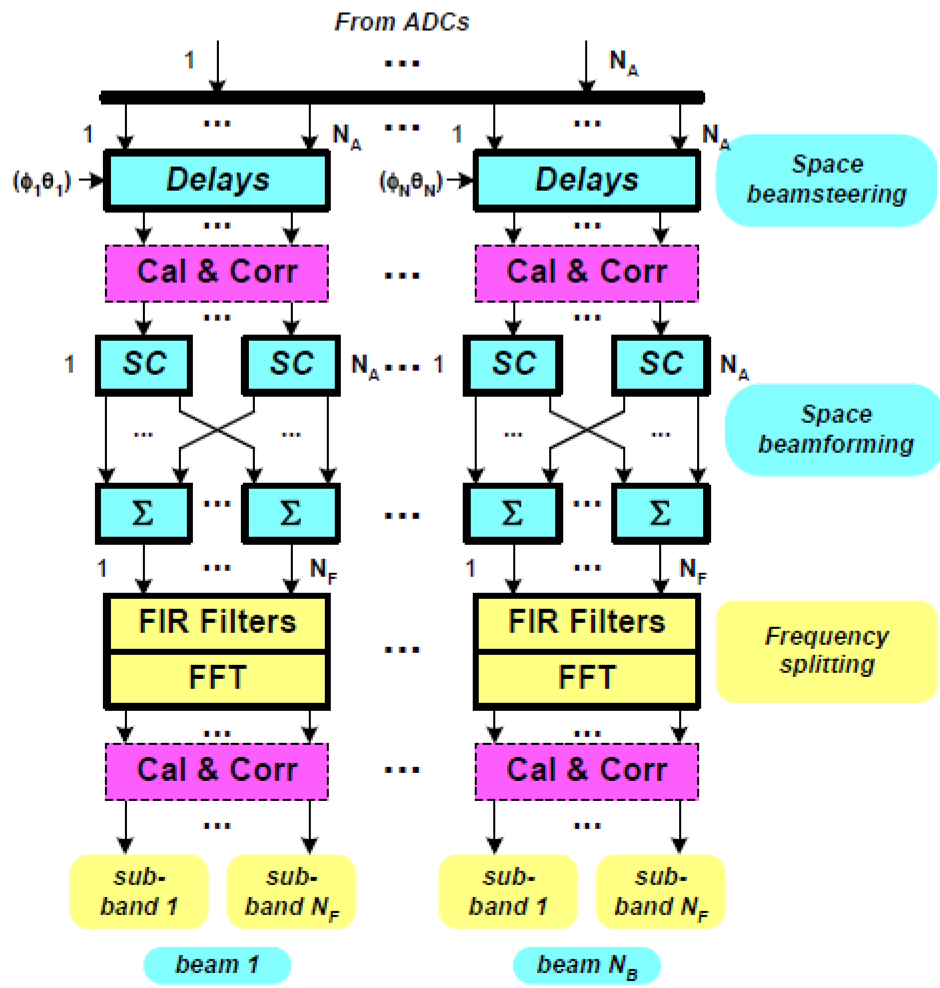
Time-delay beamforming is now an option…

Dense mid-freq array: Antenna sep ~ 20cm
Time step ~ 1ns ~ 30 cm
Angle step > 45 deg

Sparse low-freq array: Antenna sep ~2 m
Time step ~ 1ns ~ 30 cm
Angle step ~10 deg – less if interpolate

Front end unit can combine space-freq beamforming in a single FIR-like structure

Golden Rule: throw away redundant data before spending energy processing/transporting it

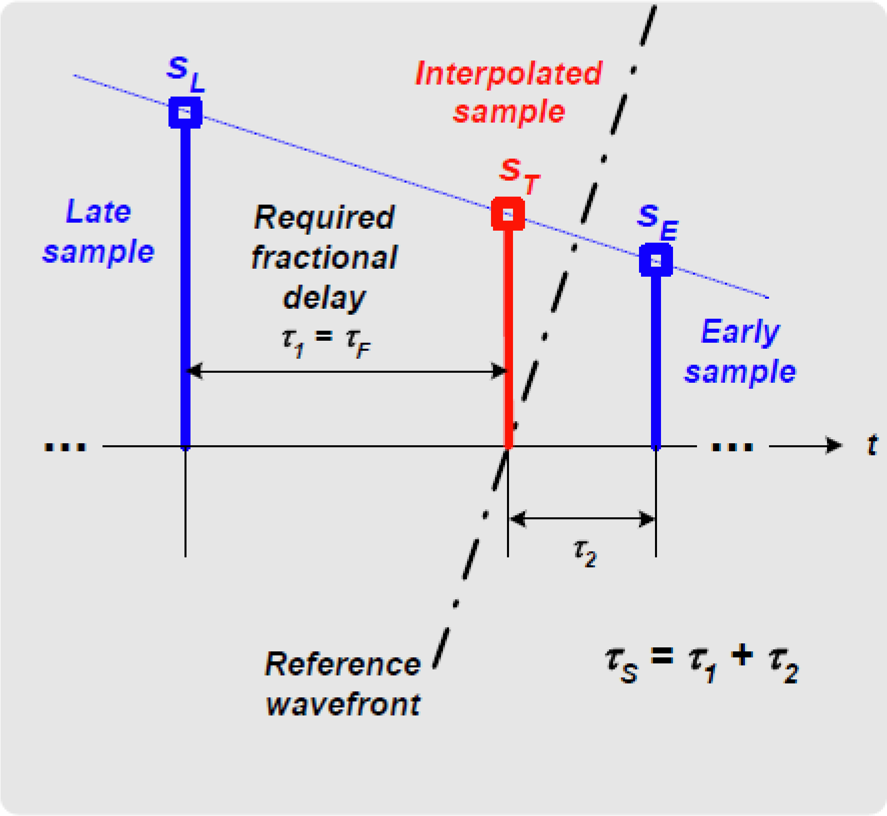


Interpolation

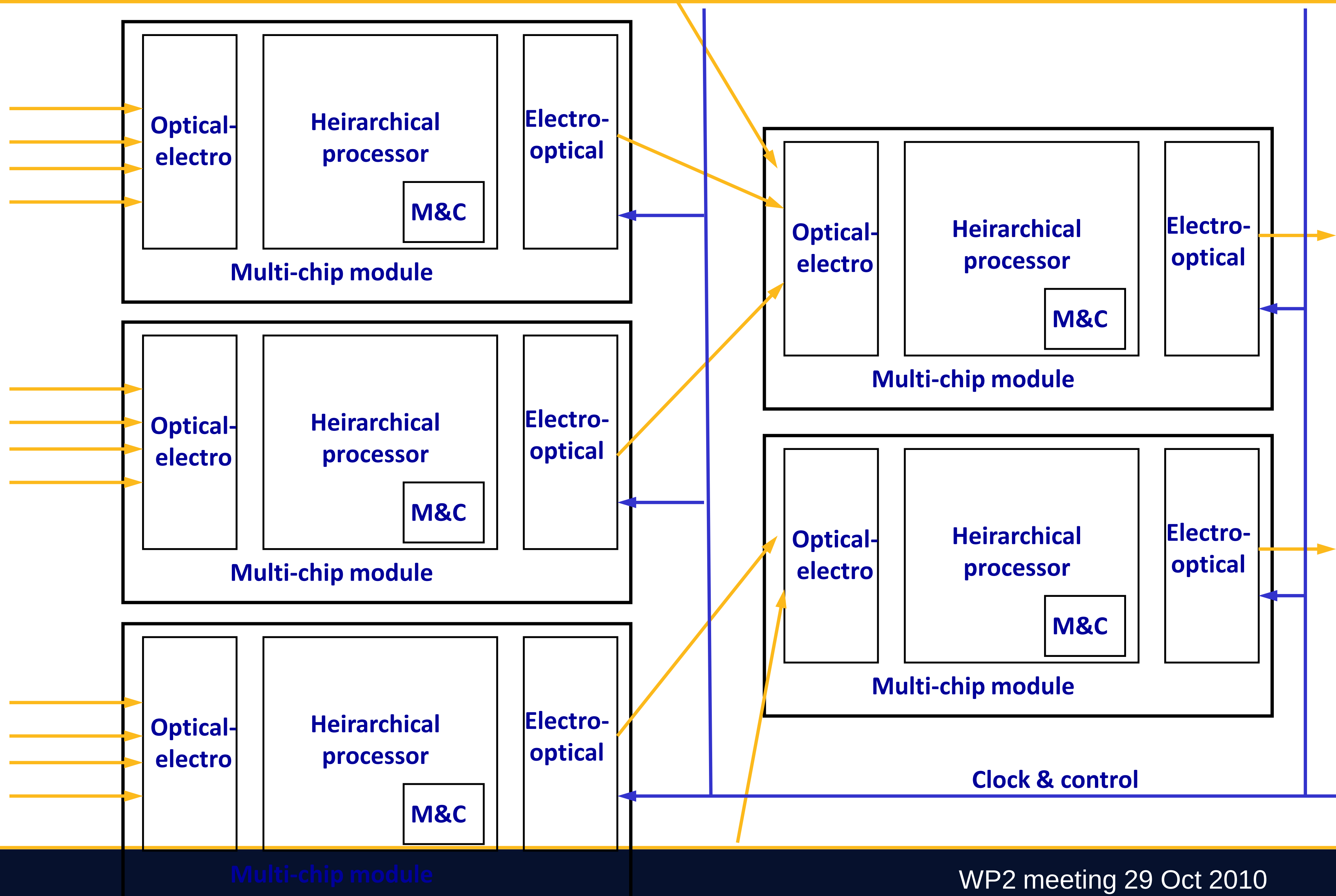
1. *Silicon gate based keyed delay banks,*

2. *FIR-filtering based, HW-level realizations consisted of FIFO structures for integer (coarse-grained) delaying and FIR filters for fractional (fine-grained) delaying,*

3. *Linear interpolation, SW-level implementations that imply re-indexing of data samples for integer delaying and time-domain linear interpolation of successive samples for fractional delaying.*



Station processor



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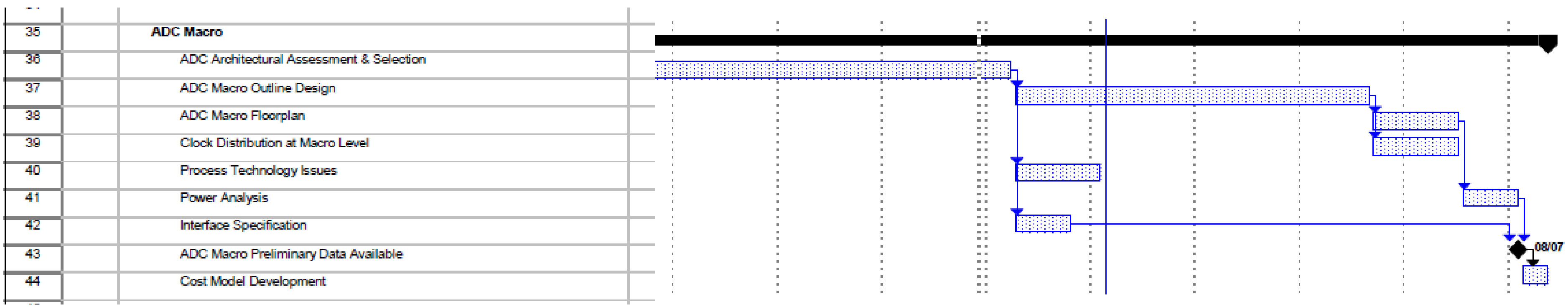
Custom Devices

- Not the intention to deliver 'finished' chip designs yet.
  - Aiming for detailed device specifications ready to start prototype manufacture when NRE money available
- There are basic engineering processes that have to be done to enable meaningful sizing, cost & power estimation
- IP identification and development – potential UK SME involvement
- Development of strategic technology partnerships
  - ADC design
  - IP macros for eg FFT, switch fabric
  - Embedded controllers
  - Non-packaged device mounting
- Identification of key architectural features
- Identify appropriate optimisation opportunities and trade-offs.
- Development of accurate models for cost and power analysis at the wider system level.
- Identify key interface 'Hot Spots' and apply effort accordingly

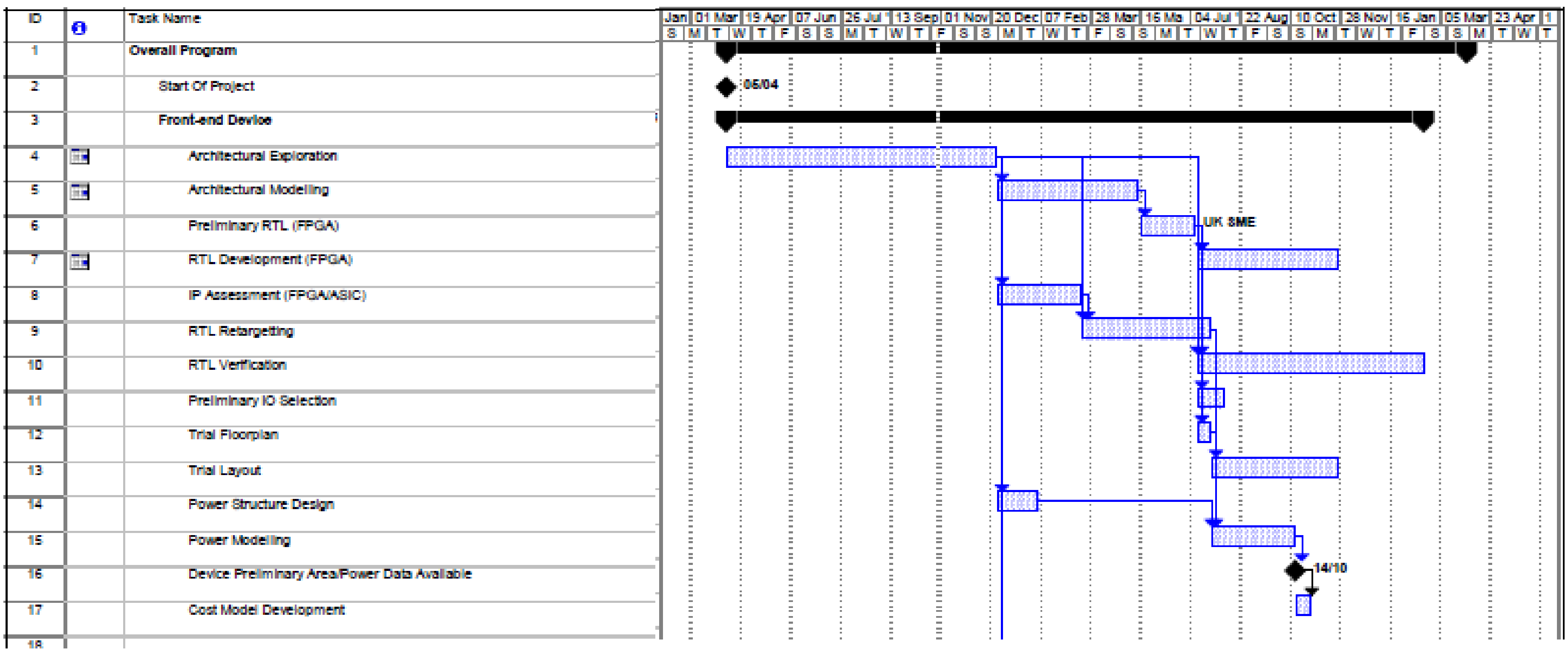
ADC Macro

- Work with specialist Industrial Partners
- Architectural Trade-Offs
- Optimisation
- Clock Coherency and Quality
- Dynamic Range and Data Growth in the data path
- Appropriate level of integration
- Semiconductor Process Selection



‘Front-end device’

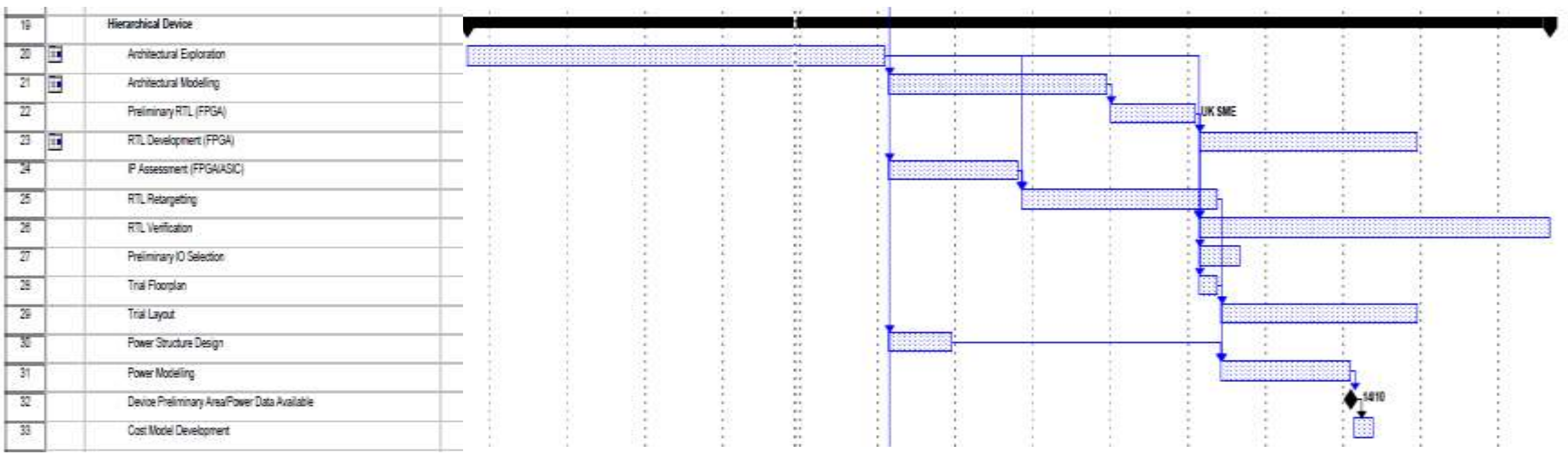
- Frequency band definition and initial band separation
- True time delay beamforming possible (just FIR filters)



ID	Task Name
1	Overall Program
2	Start Of Project
3	Front-end Device
4	Architectural Exploration
5	Architectural Modelling
6	Preliminary RTL (FPGA)
7	RTL Development (FPGA)
8	IP Assessment (FPGA/ASIC)
9	RTL Retargetting
10	RTL Verification
11	Preliminary IO Selection
12	Trial Floorplan
13	Trial Layout
14	Power Structure Design
15	Power Modelling
16	Device Preliminary Area/Power Data Available
17	Cost Model Development
18	

‘Heirarchical device’

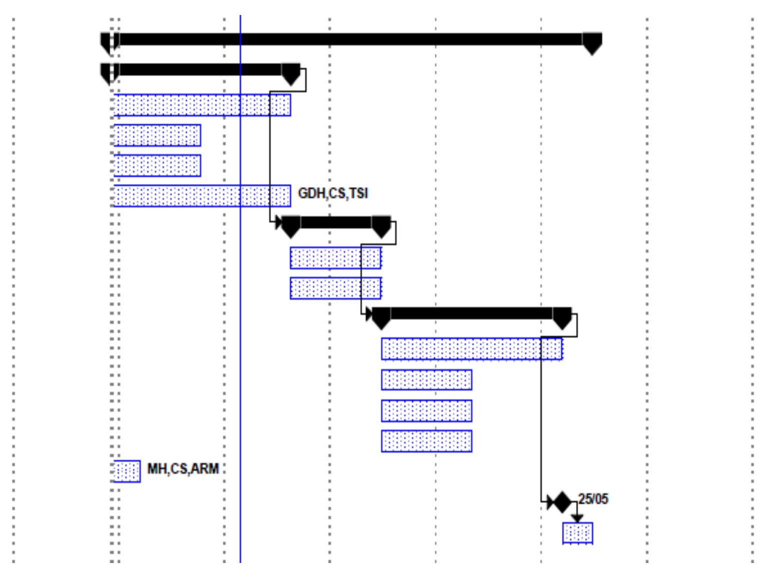
- Implements heirarchical level of beamforming
- Narrow-band beamforming – channelise and phase
- FFT/DFT TBD …(probably DFT)



Integration at Sub-System Level

- Develop industrial partnerships with skills in;
  - Design For Manufacture
  - Design For Test
  - Reliability
  - Maintainability
  - High Density systems integration
- Identification of appropriate packaging technologies.
  - Chip packages are expensive
  - Increase driven line lengths – power
  - Go for multi-chip modules
- Substrate options (FR4, PTFE etc)
- RFI Containment

46		Hardware Sub-Assembly Design Related
47		Technology Assessment & Selection
48		Interconnect Technology Assessment
49		Fibre Termination Assessment
50		Substrate Selection
51		RFI Encapsulation & Enclosure Technology
52		Design & Development
53		Power Distribution
54		Clock Distribution at Sub Assembly Level
55		Product Lifecycle
56		Design For Manufacture
57		Testability
58		Reliablity
59		Maintainability
60		Management & Control
61		Sub-Assembly Preliminary Data Available
62		Cost Model Development
63		

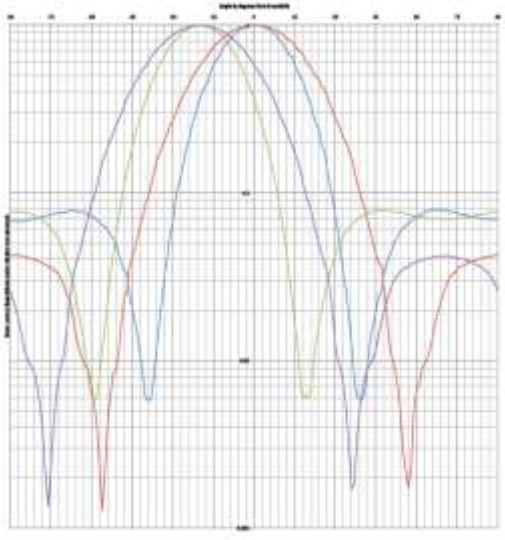


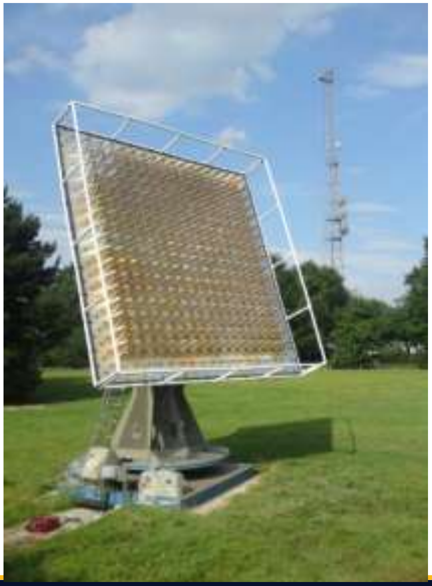
Control And Monitor at Low Levels of System Hierarchy

- Embedded Processing requirements
  - Coefficient loading
  - Monitoring and control
- Network Protocol
- Usage Cases
- Integration with higher level system M&C.
- Standards based TCP/IP
- Industry Standard processing (ARM, MIPS etc) – mobile phone technology

Prototyping

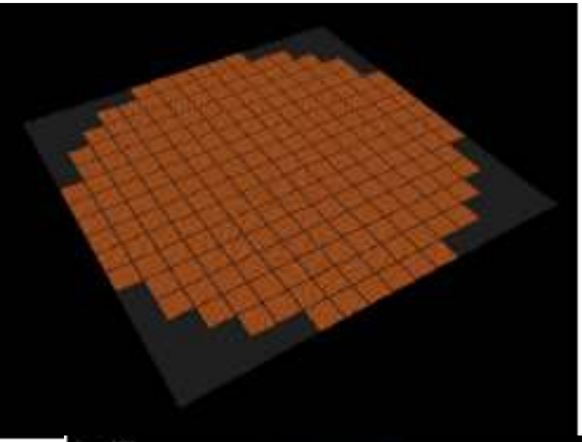
- Use existing FPGA Hardware;
  - UNIBOARD, DAQ,Casper etc.
- Small Scale subsystem tests
- Synthesis of Analogue Signals without 'Real RF Front End' – constructing an 'analogue beamformer' test-signal generator
- Design proving and Validation of Key RTL Blocks
- Design Re-Use Methodology
- Station beamforming simulation using software tools – OSKAR

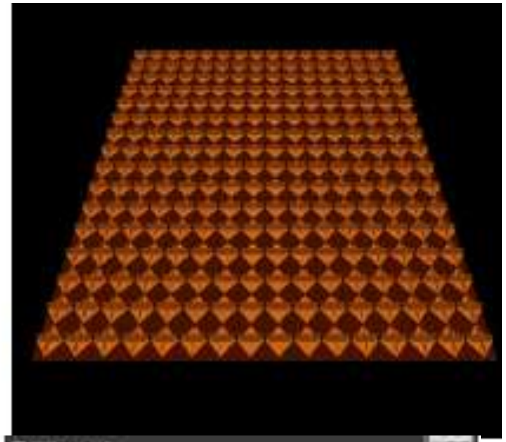




Simulation and Calibration

http://www.oerc.ox.ac.uk/resources/astro-software-repository-service





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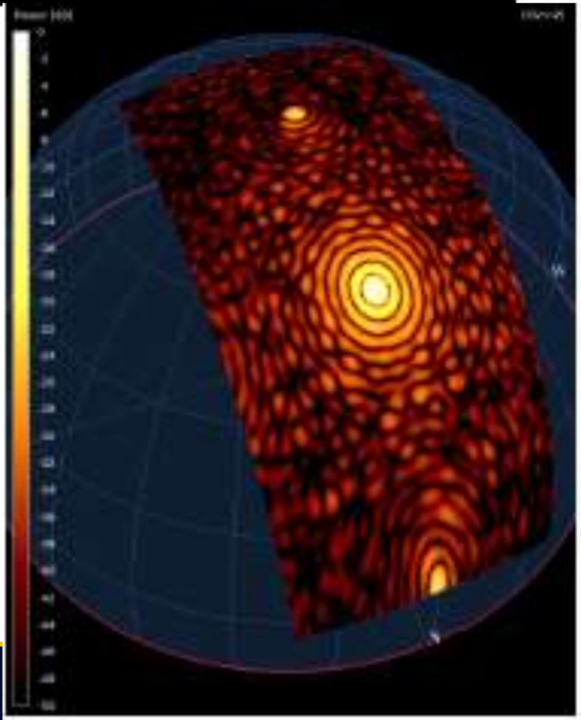

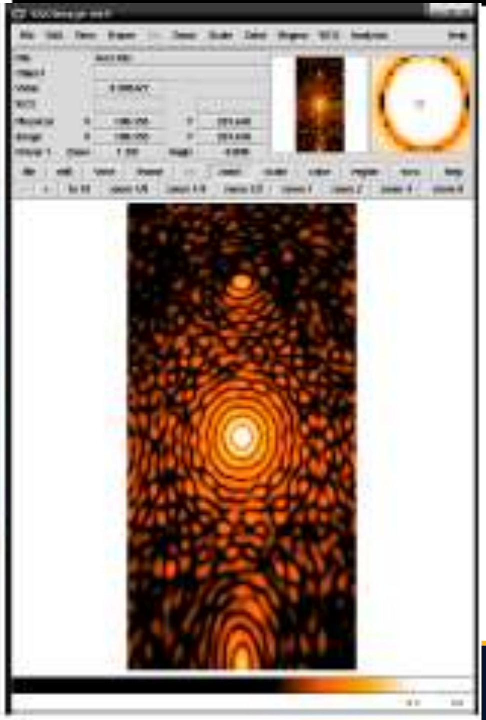

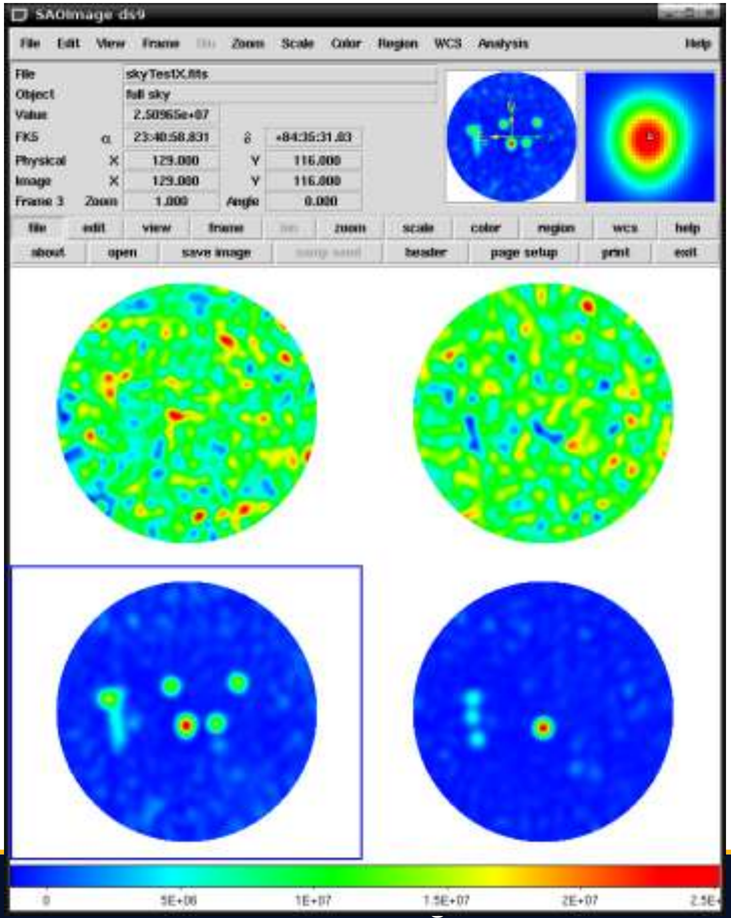

Summary

- Memo 125 specs are a big step forward…but need a lot more detail
  - Confirm outline specs against science requirements
  - Additional science-driven specs eg station/array config
  - Technical-driven specs: eg limits on data transport, correlation
- Despite this, can now make serious progress on beamforming hardware
- Programme to set chip specifications by end of PrepSKA
  - Hardware and software platforms for this in place
- Ready for prototyping during pre-construction phase

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