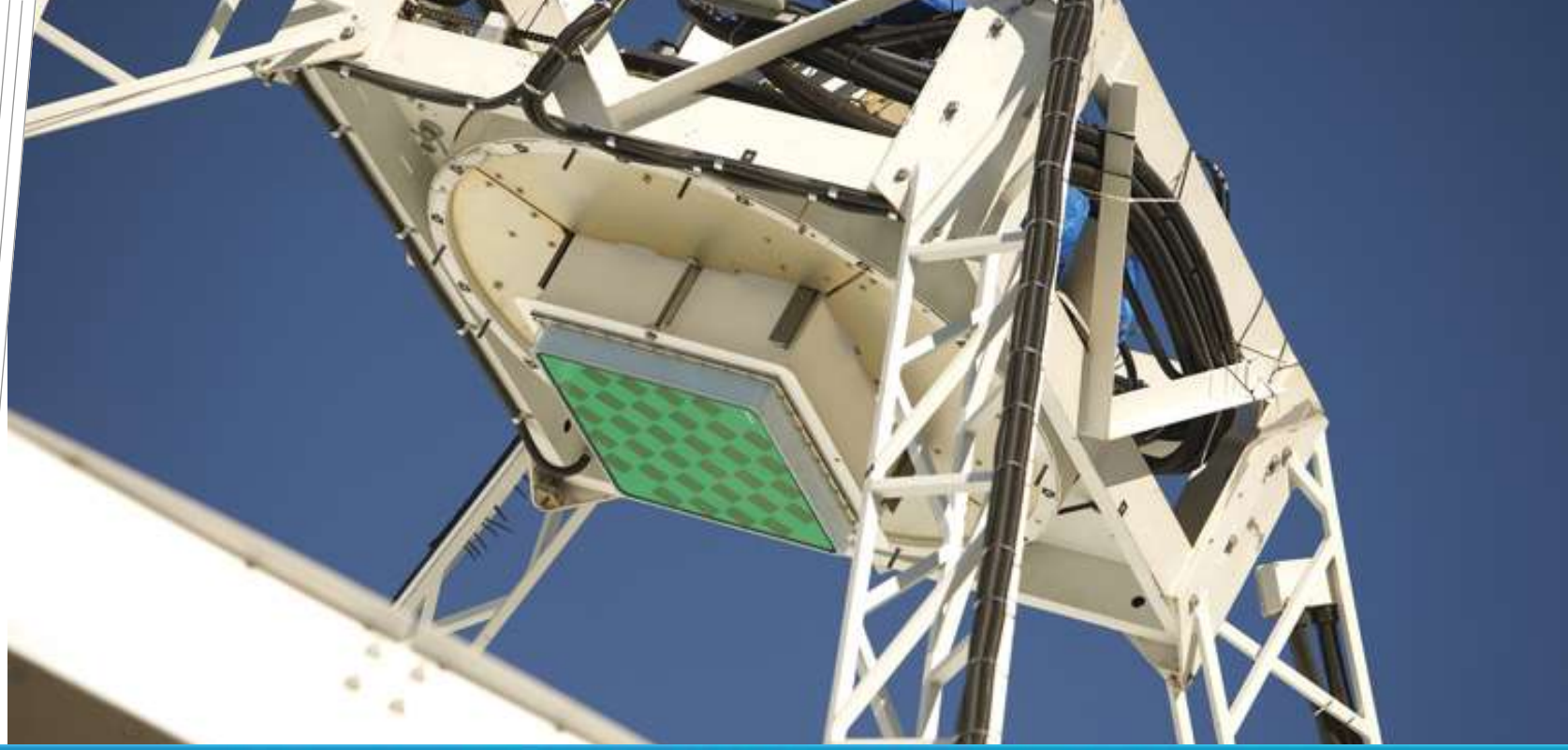

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SKA PAF Beamformers

John Bunton
CSIRO
PrepSKA WP2 Annual Meeting 2010
27-30 October 2010, Oxford

CSIRO

SUMMARY

- Beamformer Requirements
- Beamformer Topologies
- Beamformer Realisation
- ADC and Filterbanks
- Module Locations
- Current Status
  - BYU/NRAO
  - ASTRON
  - University of Calgary
  - NRC-HIA/DRAO
  - CSIRO

PAF beamformer task

- Digitise 120-200 PAF outputs (Ports)
- Form a complex weighted sum of this data to form a beam
  - Frequency dependent
- Form ~30 dual polarisation beams
  - High stability required, fraction of a degree and dB gain/minute
  - 20-40 Complex multiplies per input value (~60 if all ports used in all beams) (~500Tops/sec/GHz per PAF)
- Calibration of beam requires
  - ACM Array Covariance Matrix – correlation of every element against every other element (60-100 complex mults/input value)
    - Potentially more computation here than in beamforming
  - Correlation against calibration signal – being investigated
  - Also ADC statistics, port power spectrum
- Other function that may be implemented in beamformer
  - Filterbanks, transient buffers, fringe stopping, delay correction

Frequency Dependence

- Beam formed as

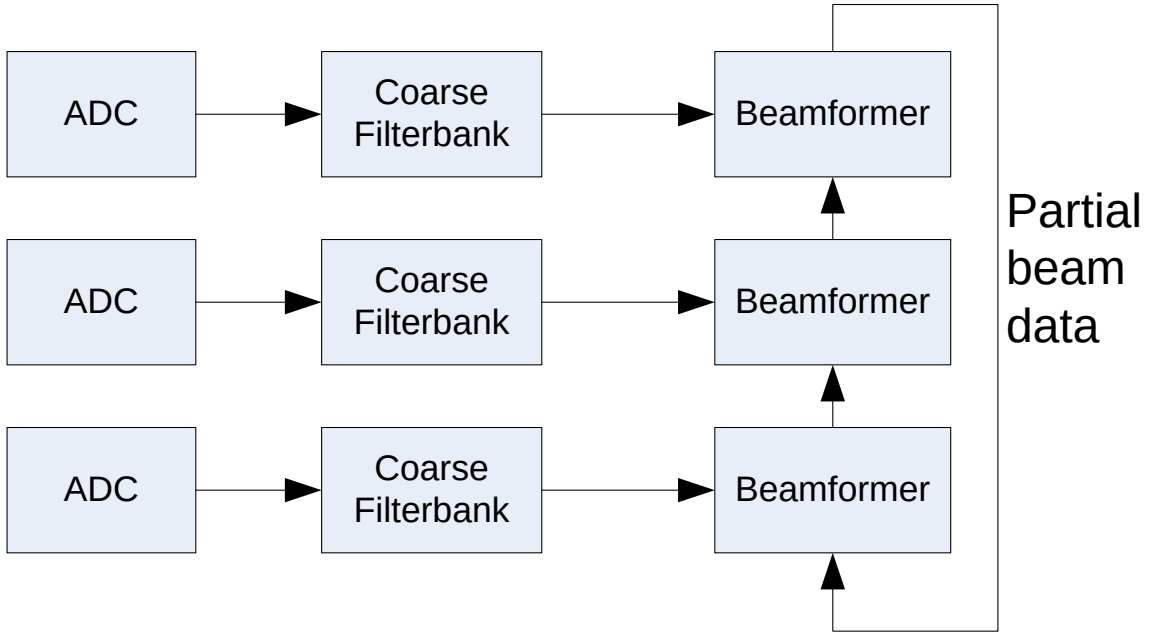
$$B(\omega) = \sum_{i=all\_ports} H_i(\omega) V_i(\omega)$$

  - Note we use the term ports as element can be single or dual pol.
  - Some of the $H_i(\omega)$ could be zero
- $H_i(\omega)$ varies with frequency due to
  - Focal spot changing size with frequency
  - LNA matching changing with frequency
  - Resonances with the FPA (can be narrow band)
  - Receiver system transfer function (fairly high order filters)
- Time domain filtering more the 40 complex multiplies per input sample
- Frequency domain filtering 1 complex multiply per input sample + FFT
- FFT < 10 complex mults/input sample AND amortised over ~30 beams
- **Frequency domain filter the most efficient**

Beamformer Topologies

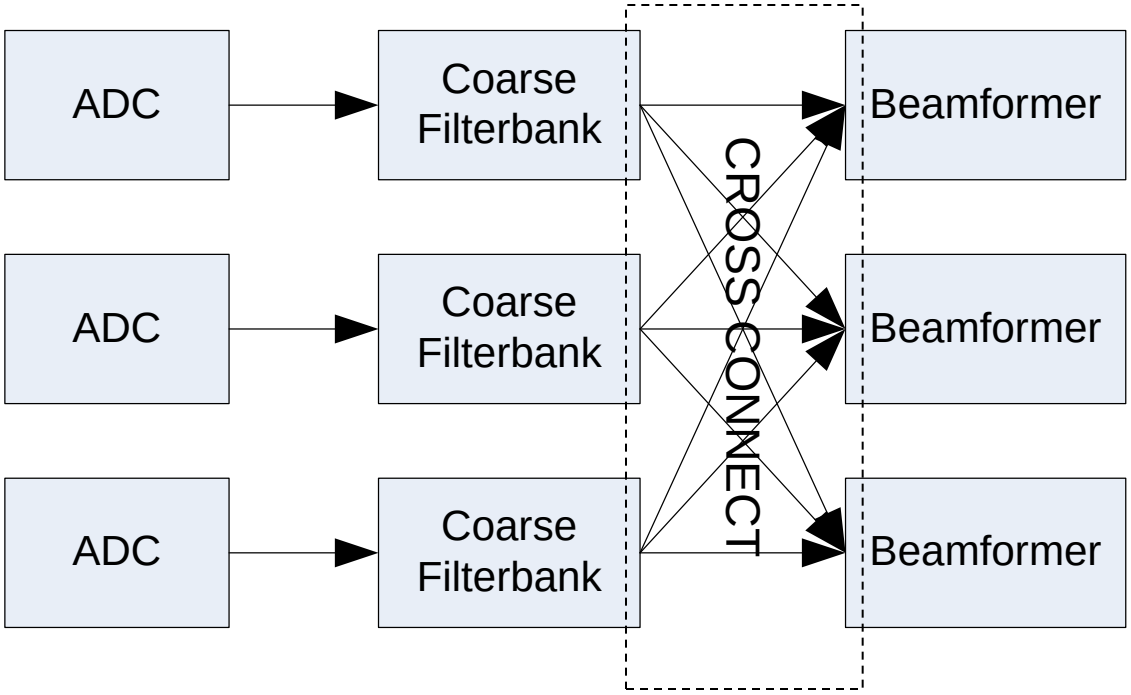
Ring Beamformer

- Data for single port to single beamformer module.
- In each beamformer module sum all available data
  - Generates partial beam
  - pass partial beam data to next module to add data from other inputs.
- N modules = N-1 transfers of part beam data



Cross Connect Beamformer

- Frequency domain beamformer requires filterbank/FFT ahead of beamforming
- After filterbank use cross connect to distribute part of bandwidth to each beamformer module



ACM (Array Covariance Matrix)

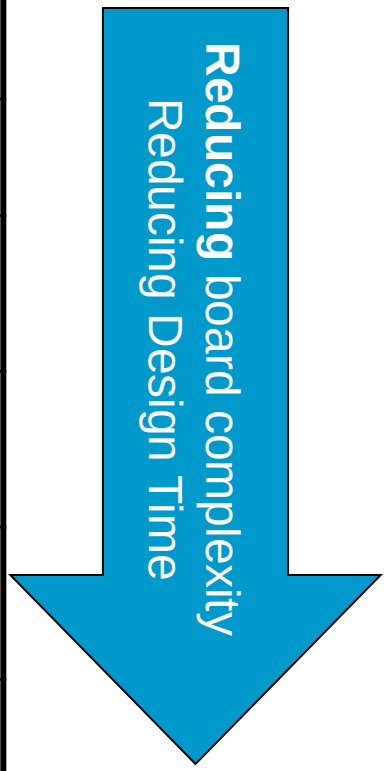
- Calculation of beam weights requires computation of ACM
- ACM has
  - Auto correlations of all ports
  - All cross correlations between ports
- N port = N(N+1)/2 correlations
- Correlations vary with frequency – compute in ~1MHz bands
- Requires all port data to be brought together for each 1MHz band.
  - Cross connect beamformer –YES
  - Ring beamformer – NO (other data paths needed)

- ACM requirement pushes design towards cross connect beamformer

Beamformer Realisation

Board Design Philosophy

Project	FPGA Family	FPGA Size	Multipliers	#FPGAs per board
MOPS	Virtex-2 VP30	120nm	2000	17
SKAMP/MWA	Virtex-4 SX-35 +	90nm	1700	14
CABB	Virtex-4 SX55 VP2-50	90nm	2000	10
ASKAP Redback1	Virtex-5 SX95	65nm	2600	5
Redback2	Virtex-6 LX240	40nm	3000	5
Redback?	Virtex-7/StratixV	28nm	8000	5



Beamformer Compute Requirements

- Specification for beamformer not properly determined yet
  - 36 beams
  - ~100 inputs to form each beam (not all ports per beam)
- Bandwidth requirements
  - SKA_2 guess 750MHz (for example 0.45-1.2GHz)
  - SKA_1 guess 300MHz
- 36 beams x 2pol x 100 inputs x 300MS/s = 2 T CMAC/s
  - CMAC = Complex multiply accumulate
- Full ACM for 200 ports (200x201/2) correlation by 300MHz =6T CMAC/s
- ACM could dominate but only needed for calibration
  - Variation slow – compute with lower sensitivity
  - Use part of bandwidth and/or time samples
  - ASKAP computes 1/5 bandwidth and 1/4 time samples
- ACM computation 15% of beamforming compute load
  - Total ~2.5T CMAC/s

Beamformer Size

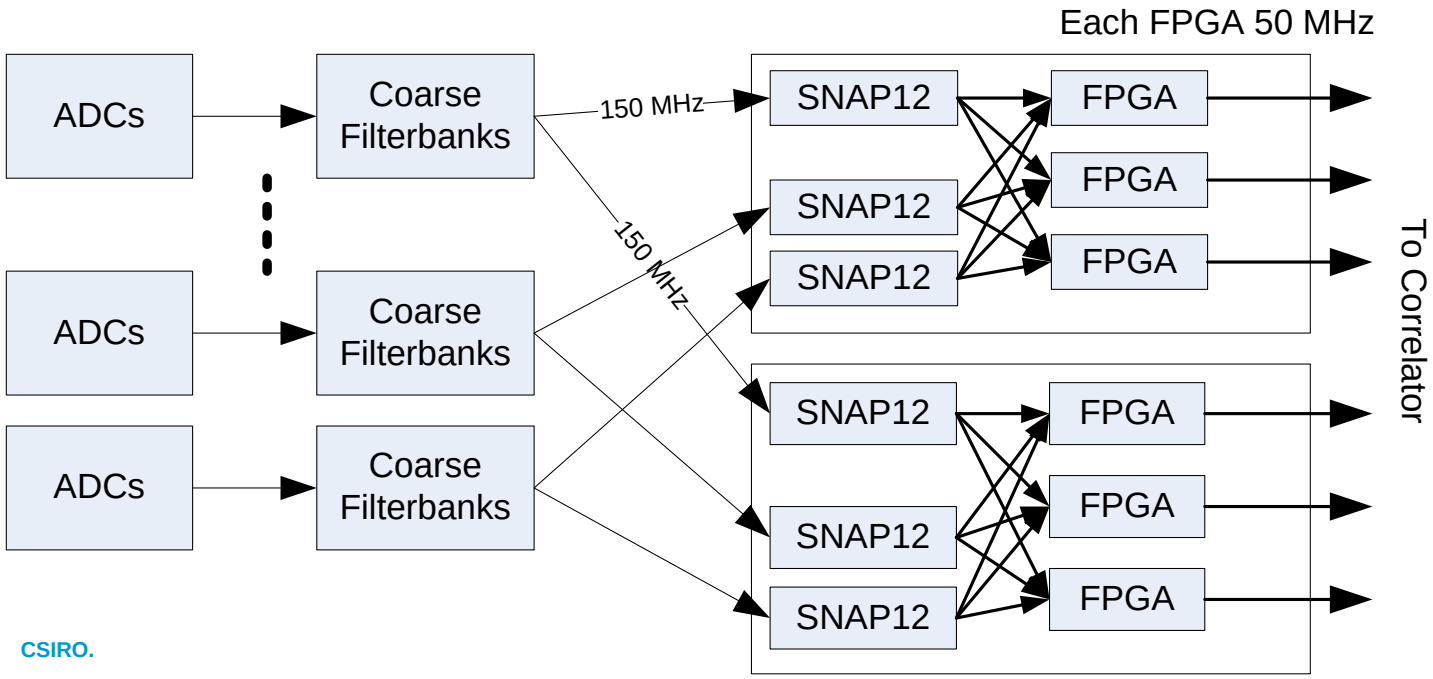
- In 2012 midsized FPGA has 2000 multipliers at 300+MHz
  - 150G CMAC/s (Complex Multiplies Accumulates/s)
  - SKA_1 requirements ~2.5T CMAC/s = ~16 FPGAs
- FPGA performance approximately doubles every 2 years
  - 8 FPGA sufficient in 2014 for SKA^1
  - 4 FPGAs sufficient in 2016 for SKA_1
    - Three more generations (factor 4 more performance)
    - Hafnium dioxide dielectric has solved most leakage problems for these
- Beamformer will consist of 1 or 2 processing boards
  - Plus ADC/coarse filterbanks system

Beamformer Module I/0

- Each port >750MS/s of complex data and >8+8bits
  - More than 12Gb/s per port
- Up to 200 ports
  - More than 2.4Tb/s into beamformers
- Technology to move this data at low cost
  - Currently SNAP12 technology (Agilent PONI) lowest
    - 12 fibre ribbon cables and 12TX and 12RX modules
    - 6.25Gb/s per fibre and increasing but short range (less than 1km)
    - 2018 transport up to 10 ports per SNAP12 connections
    - At least 10 SNAP12 modules for input, (100GE for output?)
- Suggest 2 beamformer board – 3 FPGAs and 5+ SNAP12
  - Simpler board and simplified cooling compared to single board
  - Design easily extends to 1GHz bandwidth
- Future alternative 100GE – 4 fibres at 25Gb/s each
  - Up to 8 ports per connection (but input and all output catered for)
  - Each board has ~7 100GE connections

Possible Beamformer Architecture

- Number of ADC/Coarse filterbanks systems
  - Number equal to number of SNAP12 inputs (~5)
    - If Beamformes and ADC separated
- Half bandwidth to each beamformer board
- SNAP12 to 3 FPGAs – data for each FPGA on 4 fibres
  - No interconnections between FPGAs (Favours cross connect over ring)



ADC and Filterbanks

Down Conversion or Direct Sampling

- SKA fractional bandwidth up to 100%
- Then maximum frequency is 3X minimum frequency (.5-1.5GHz)
- ADC in first Nyquist zone (DC to Fs/2) use 2/3 of available data

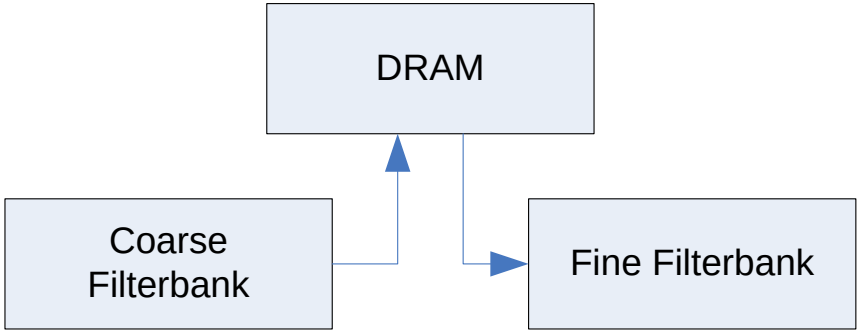
- Conclusion wide fractional bandwidth then
  - Down conversion not required – direct sample in first Nyquist zone

- For smaller bandwidth, sub-octave
  - Maximum frequency is 1.8X minimum frequency
  - eg 0.7 – 1.25GHz, unlikely to want less for HI science
  - Operate ADC in second Nyquist zone (Fs/2 to Fs)
  - Again no down conversion needed

- ADC will directly sample RF for HI science

Filterbank Implementation

- Large filterbanks store data and coefficients from RAM
- FPGAs have multipliers and RAM in ~1:1 ratio
- Maximum on-board filterbank size limited by RAM size
  - Beyond ~2k filterbank RAM is limiting resource – multipliers are underutilised
- SKA calls for ~100k frequency channels
  - Single stage filterbank underutilises multipliers by order of magnitude
- Solution two stage filterbank (used in SKAMP,MWA,CABB,ASKAP …)
  - First stage coarse oversampled filterbank,
  - Frequency resolution ~1MHz, suitable for beamforming
  - Second stage fine filterbank to final frequency resolution (~1kHz)
    - Third stage for resolution less than 1kHz



Coarse Filterbank

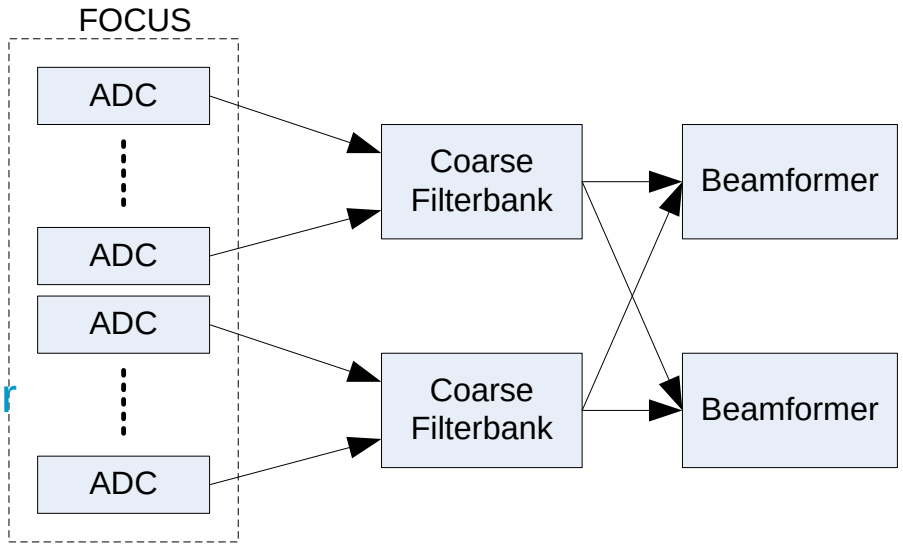
- Oversampling polyphase filterbank
  - ~20 real multiplies per real input
- 200 ports at ~2GS/s (0.75-1 GHz bandwidth)
  - Computation 200 ports x 2GSamples/s x 20 multiplies/Sample
  - 8T real multiplies/s
- FPGA in 2012 – 2,000 multipliers at ~300MHz (mid size)
  - 0.6 T real multiplies/s
  - 4 times as much in 2016
  - Could do all filterbanks with two FPGAs
- If ADC data outpus
  - need ~20 SNAP12
  - Use 4x25G links (100GE) ~25 links
- If ADC on filterbank board
  - ADC likely to be a quad device – up to 50 ADCs

✓ADCs determine number of boards/FPGAs

Module Locations

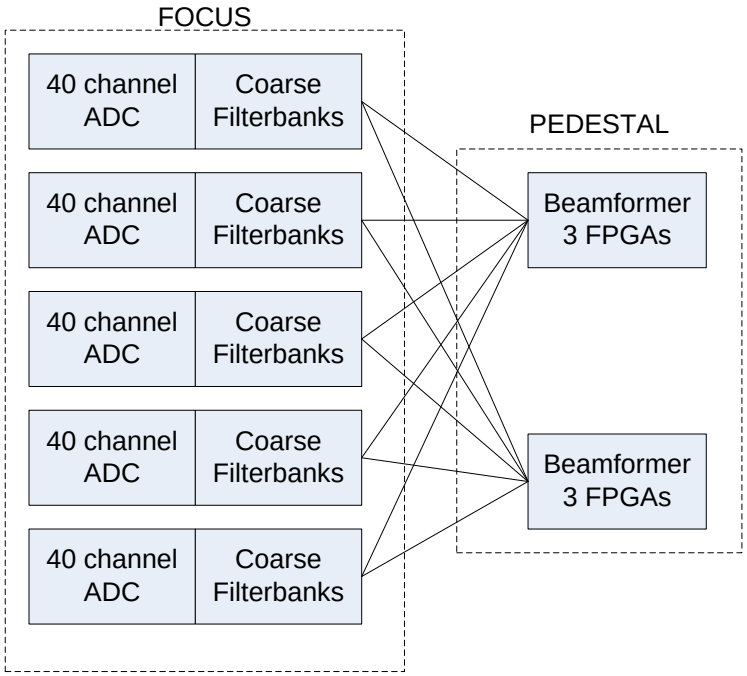
ADC separate from filterbank

- ADC separate from filterbanks implies three subsystems
  - ADC, Filterbank and Beamformer
- More systems generally means higher cost and more data transport paths.
- But may be possible to have ADC at the focus within the PAF
- Prefer combined ADC and laser driver for high speed serial link (UCalgary)
  - 1-2 fibres per ADC port,
  - Use SNAP12 technology 16-32 ribbon cables to thread through cables wraps
- Possibly two coarse filterbank boards 100-200 optical inputs each
  - 8-16 ribbon cables
- Cross Connect in same shelf to beamformer boards
- Location of filterbank/beamformer
  - Pedestal
  - Station building
  - Central site



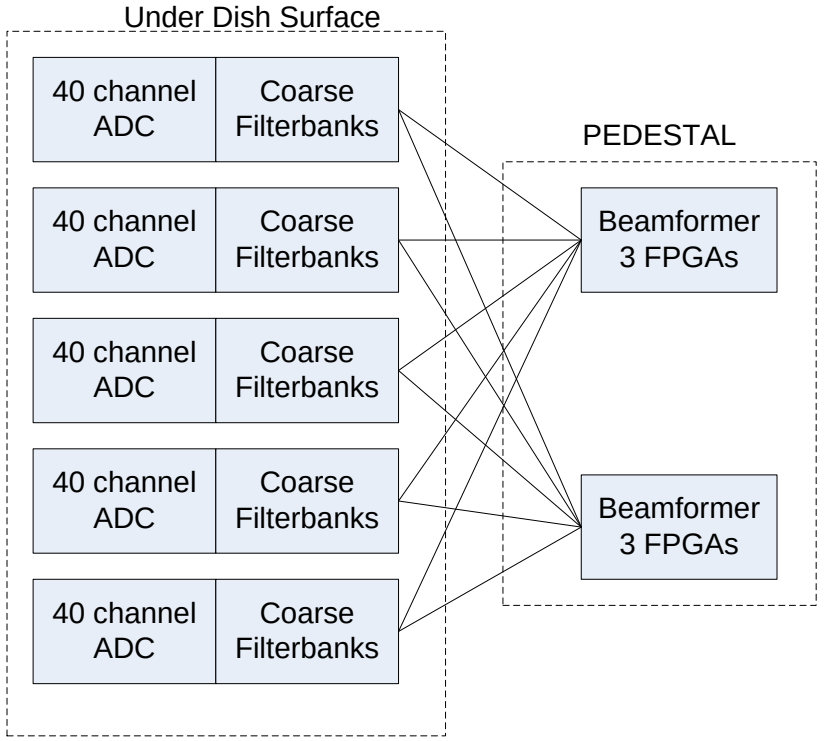
ADC with filterbank

- Can ADC combined with coarse filterbank and located with PAF at focus
- Say 40 ADC ports per board
  - 4-5 boards
  - ~10 quad ADC per board and one FPGA
  - 4, 6 or 8 12 fibre SNAP12 links per board
  - Half of SNAP12 cables to each of the beamformer boards
- Cross connect to beamformer in pedestal implemented with cabling from focus
- Fewest modules types
- But more electronics at focus.
- Test have shown processing within FPGA generates little RFI
  - No major RFI penalty
- Cooling, weight and space major constrains wrt to just ADC at focus



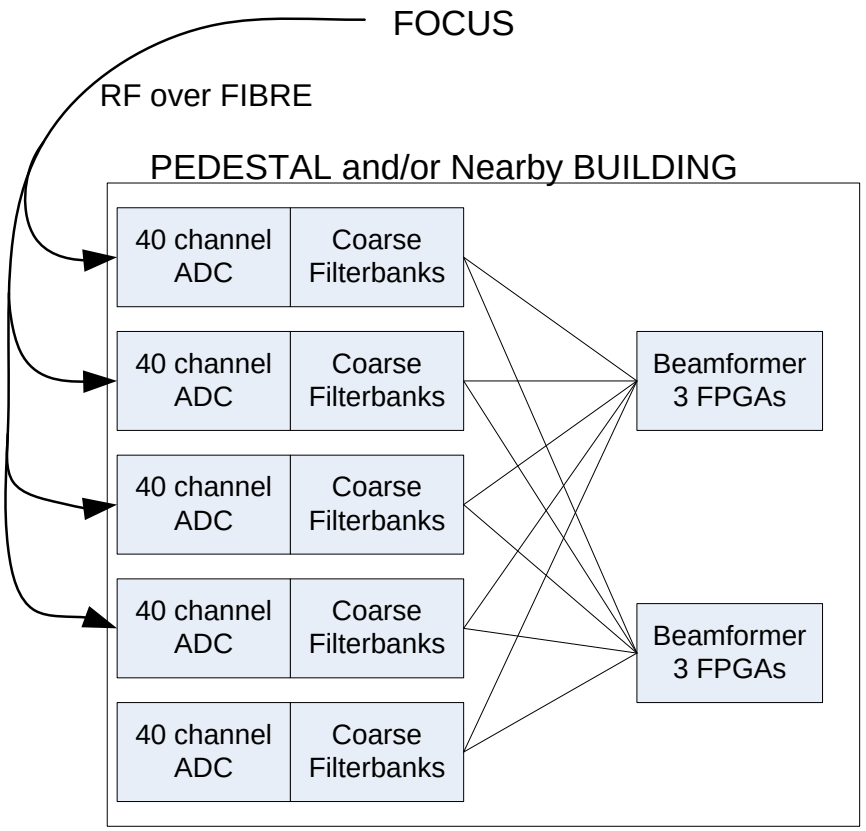
ADC under Dish Surface

- If RFI, heat, size or weight too great must move ADC from focus
- Analogue over Coax to pedestal is not practical for SKA
  - High loss
  - Difficult to implement cable wraps
  - High cost over $100 per coax
- But Coax to underside of dish surface may be cost effective
  - Better RFI performance
  - Greater separation from PAF
  - Shielding provide by dish surface
  - Heavier RFI shielding possible
- ~10m of coax
  - Acceptable cable loss
  - No cable wraps
  - Some added cost



ADC in Pedestal (or nearby)

- To move ADC to pedestal or nearby building use RF over Fibre
  - Up to 10s km
  - Dynamic range? - improving
- RF over fibre is an added cost
  - But simplified maintenance, cooling, access
  - Together with better RFI shielding and lower weight at focus
- Still have ADC and coarse filterbank combined
  - Lowest cost digital electronics
- Cross connect to beamformers may still be optical to provide isolation

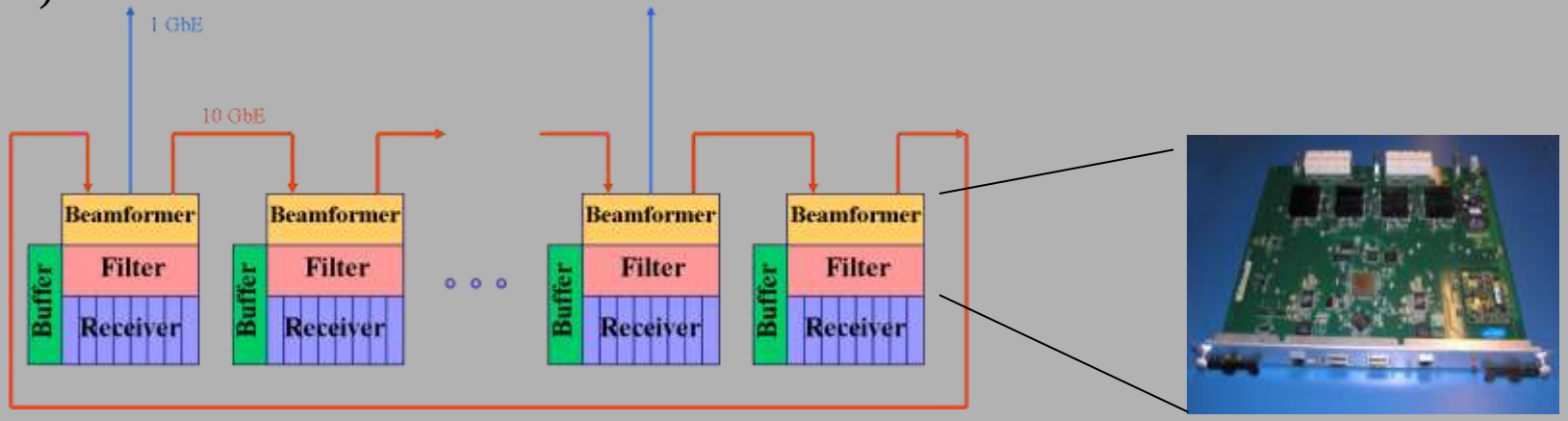


ASTRON

Andre Gunst

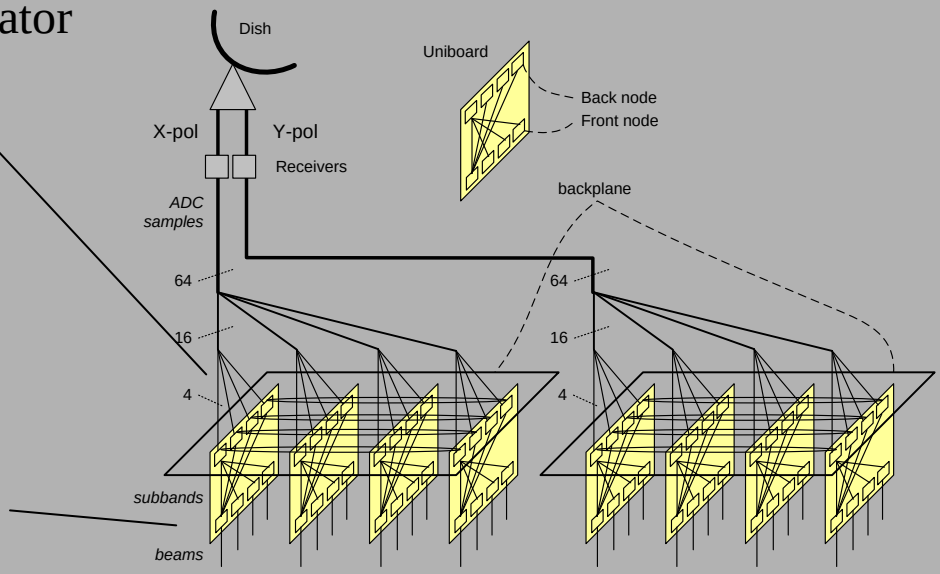
LOFAR Station Beamformer

- Distributed beamformer
- Locally a partial sum is calculated and passed (red arrow) to neighbor
- Four boards are responsible to sent final data product (blue arrows)
- Weighted sum over 96 dual pol. signal paths
- One second update rate
- On the fly correlation done for all 192 signal paths per subband (1 s)
- Gain and phase corrections are included in beamformer weights
- Bandwidth: 48 MHz (split in 248 subbands of ~195 kHz each)
- Bandwidth can be exchanged with # beams (beam of 48 MHz, 2 beams of 24 MHz, etc.)



APERTIF Beamformer

- Multiple UniBoards combined via a midplane (dense solution)
- 8 receivers with 8 ADCs each connected to other side of midplane
- Front node FPGAs split bandwidth
- Back node FPGAs do the beamforming
- Transpose done partially on board and backplane
- Weighted sum over 61 signal paths per telescope
- Output bandwidth: 300 MHz
- Number of beams: 37
- 96 UniBoards required (12 telescopes)
- Connected via fiber to APERTIF correlator



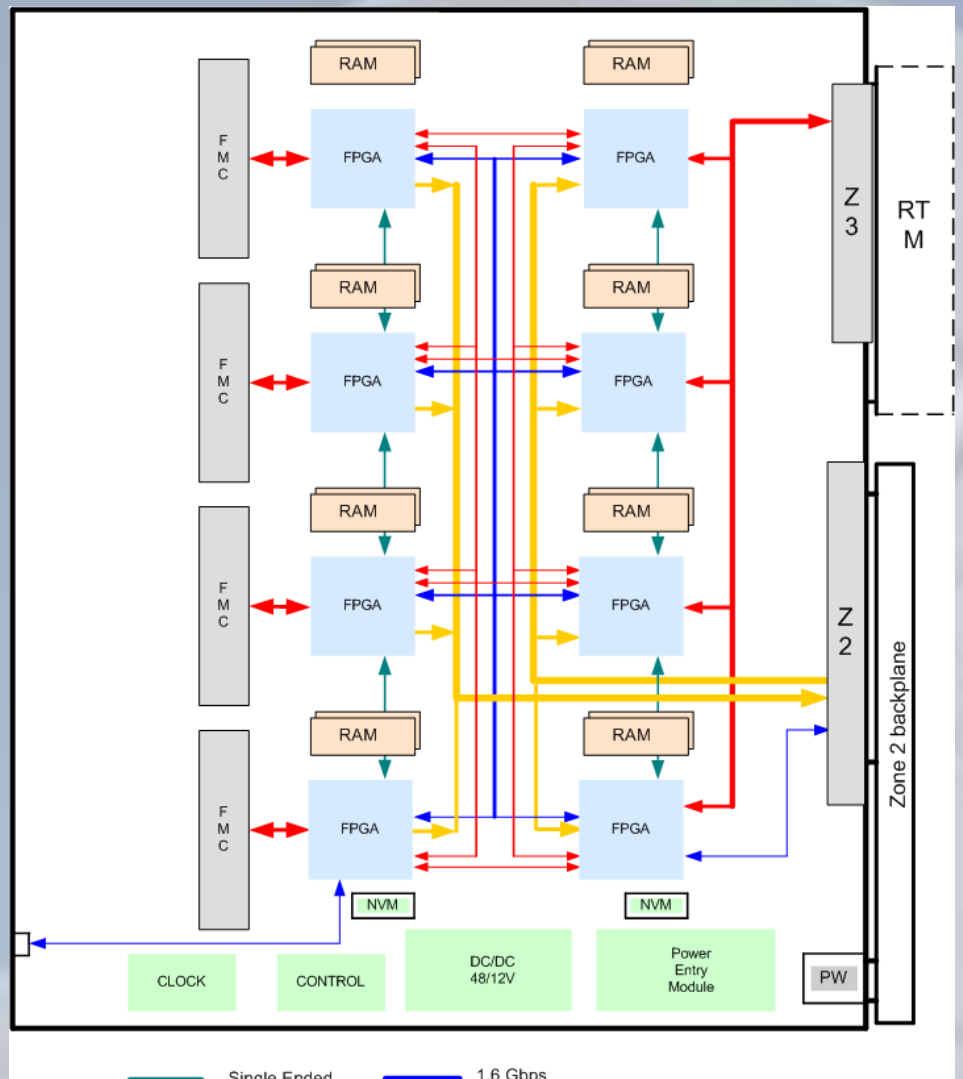
NRC-HIA/DRAO

Zoran Ljusic

Zhang Heng

NRC·CNRC
Herzberg Institute of Astrophysics
Dominion Radio Astrophysical Observatory

DRAO Octal Blade Beamformer System



- Supports broadband beamforming adaptive optics real-time control (Tomography)
- Eight Xilinx FPGAs per board (8 TMACs)
- 16 RAMs per board, 2 per FPGA (128 GBps total)
- AdvancedTCA Chassis (Z2 150 Gbps ; Z3 160 Gbps)
- Four FPGA Mezzanine Cards for I/ (160 Gbps total)
- Layout underway. Prototype mid-2011

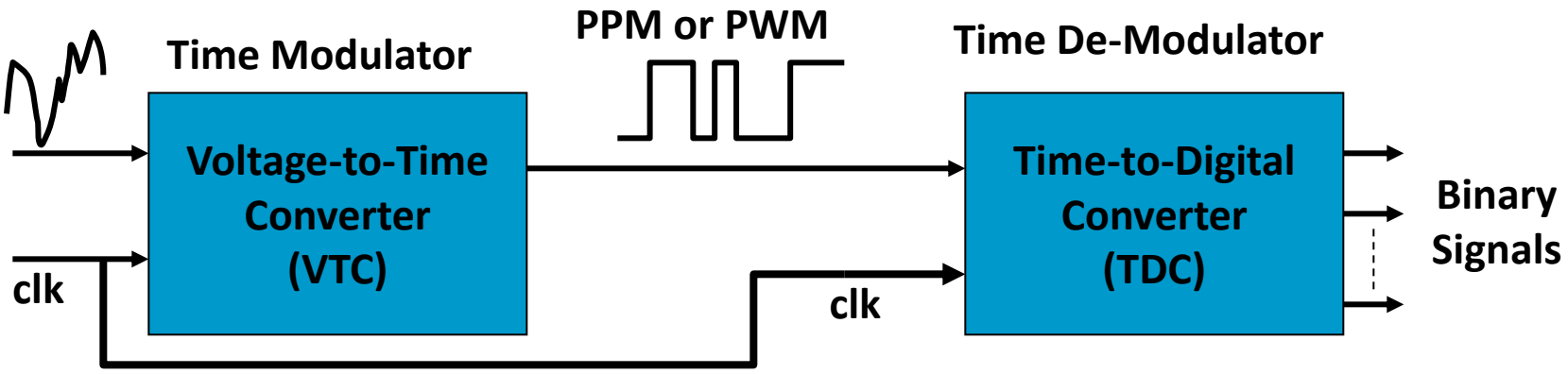
University of Calgary

Jim Haslett

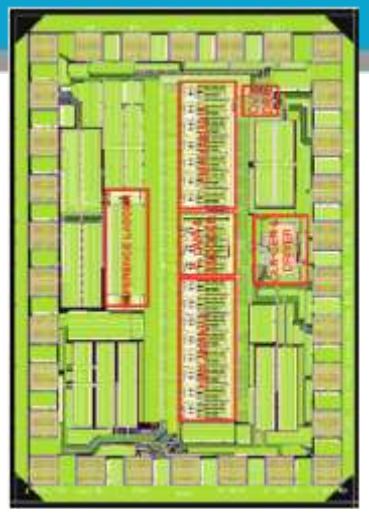
Leonid Belostotski

University of Calgary ADC work

- Working on high speed low power CMOS ADC's.
- Two approaches are investigated
  - Flash ADCs
  - Time based ADCs: Time based ADCs consist of two sections that can be separated. In that configuration the VTC could be located at the antenna and the TDC at the data processing unit (no SerDes required)

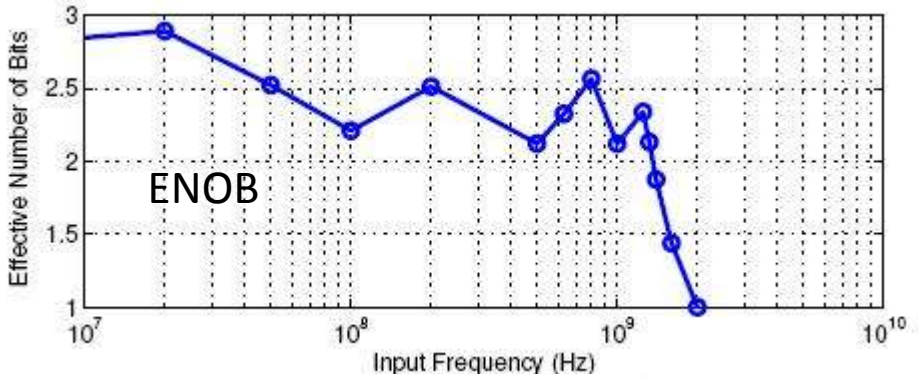


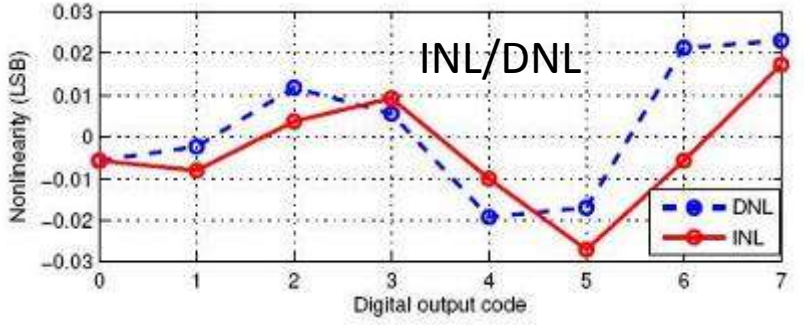
University of Calgary ADC work



- Flash ADC Status:
  - A 6bits, 10mW, 2GS/s ADC has been submitted for fabrication in 65nm LP CMOS. This ADC is self-calibrated.
  - Work started on a 6bit, 5GS/s ADC in 65nm GP CMOS

- Time based ADC status:
  - Measured 3bit, 13mW, 2.5GS/s ADC in 90nm CMOS
  - Currently working on self-calibration circuits





Brigham Young University

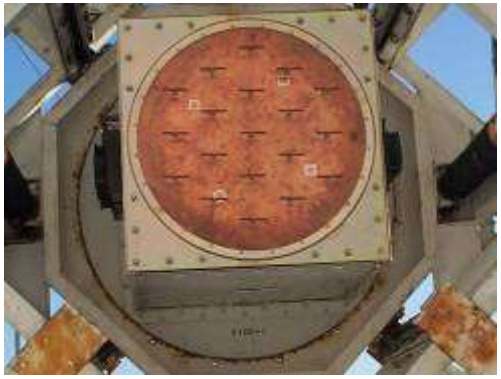
NRAO

Brian Jeffs

BYU/NRAO L-Band PAFs

2006-2007:

- 7 element array on 3m reflector
- RFI mitigation experiments
- 19 element on Green Bank 20m
- 150 K T_{sys}



2008:

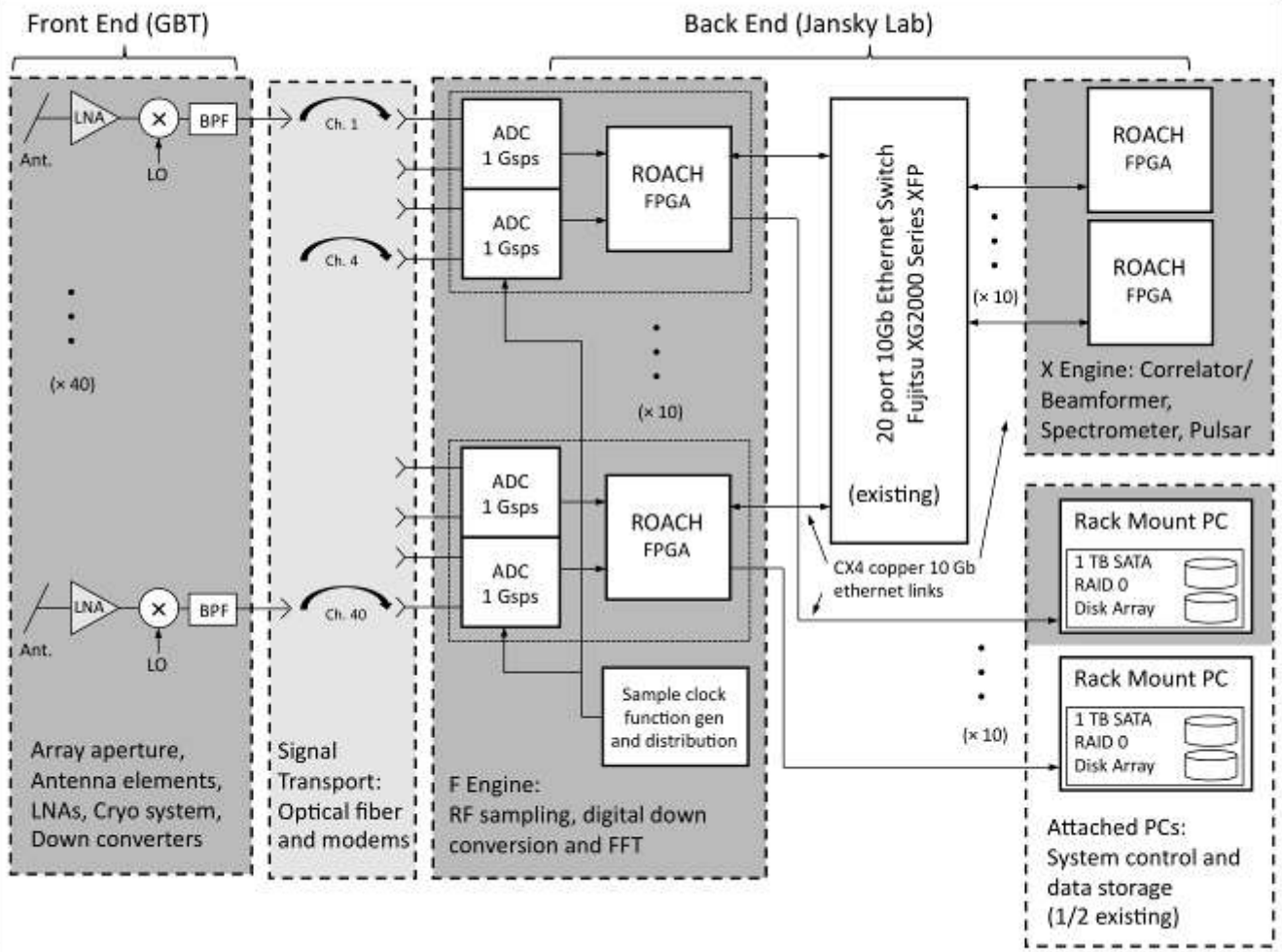
- 19 element dipole array
- 33 K LNAs (room temperature)
- 1.3 – 1.7 MHz tunable bandwidth
- *Goal:* highest possible sensitivity
- 66 K T_{sys} with room temp LNAs

2009-2010:

- Active matched low noise PAF designs
- Dual polarized 19 element array
- New 40 channel down converters and data acquisition system
- Improved beamformer methods
- Progress towards cryo-cooled array
- Deep nulling interference canceler
- AO-40 experiment on the Arecibo dish

Correlator-Beamformer Back End

- 20 CASPER ROACH FPGA boards.
- 300 MHz BW per antenna
- 40 antenna channels
- Supports 19 element dual pol array
- 40 real-time simultaneous beams
- Correlation for calibration uses selected frequency subbands.



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ASKAP

- 188 port beamformed
- 300MHz bandwidth within 700 to 1800MHz band
- Up to 36 dual pol beams (30 sq deg at 1.45GHz)
- Major risk is the chequerboard array and its performance
  - Chose to take low risk approach to many other parts of the system

- RF over coax from the focus to the pedestal
  - Manageable weight and cooling problems at the focus
  - Low cost RF over fibre not sufficiently mature at the time
- ADC and coarse filterbank in pedestal
- Beamformer with correlator at central site
  - Original design 2008 technology
  - Not enough space in pedestal for beamformer

ASKAP Hardware

- Original design used Virtex 5 FPGAs (ES1), upgraded to Virtex 6 (ES2) when they became available.
- Complete ES1 built and firmware trialled. Now abandoned for ES2 – higher performance, lower cost and most importantly only one set of firmware to support.
- Two complete ES2 systems being built now
  - When verified parts ready for build of next 4
- Two main processing boards
  - DragonFly2 – 4 channel ADC, FPGA and quad 10G optical
  - Redback2 – Beamformer, ATCA based

DragonFly system

- Command/Control and Power system moved to separate boards
  - Power, Command, Control and Timing distributed via backplane to DragonFly Board
- DragonFly-2
  - 2 Dual channel 8-bit ADC – Four coaxial inputs + 768MHz clock
  - Virtex 6 LX130T FPGA for carsefilterbanks
  - Four SPF+ optical links – each transporting 76MHz bandwidth for all four ports
- Full system
  - 48 Dragonfly-2
  - 4 Control
  - 4 Power
  - In 4 3U racks

Redback system

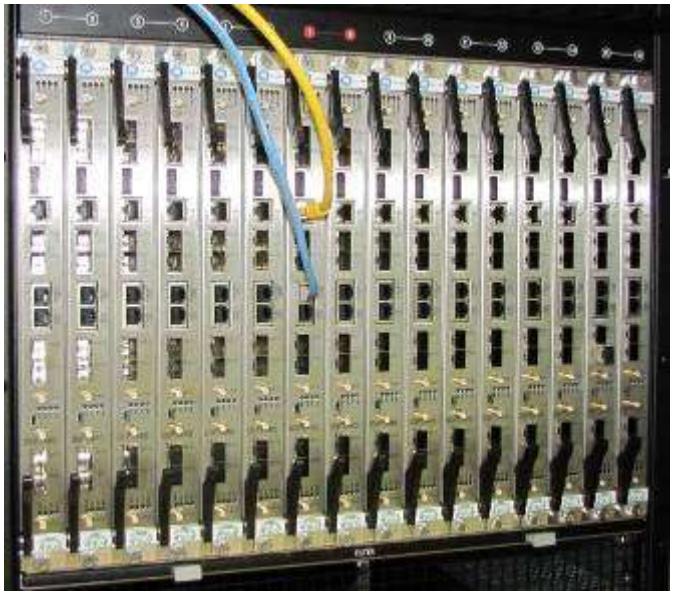
- Base on industry standard AdvancedTCA shelf with fully cross connected back plane
- 12 10G inputs to RTM
- To Crosspoint Switch to backplane
  - Data from single Dragonfly2 distributed to 16 Redback2 – 19MHz each
- Redback-2 has 4 LX240T processing FPGAs 19 MHz bandwidth for all ports)

RTM

Redback-2

AdvancedTCA shelf

Beamformer or correlator shelf



ASKAP Status and Lessons

- Second Rev of Version 2 hardware
- Two full systems under construction, four ready to go
- Dragonfly Firmware complete and cut down Redback beamformer for testing

- Demonstrate real-time beamforming on SKA class PAF
- Demonstrate 2Tb/s data transport filterbank to beamformer
  - But 192 fibres connection – must be reduced
    - Need low cost 100G for long haul, possibly SNAP12 for <1km
- Construction cost too high for SKA
  - Need to reduce number of boards
    - No separate interface boards
  - Higher I/O and processing per board
    - Need three more increments due to Moore's Law

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Thank you

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