Commercial Availability & Testing (COTS MMICs)

- **GaAs pHEMT and HJFET Low Noise Transistors**
- **Noise Figure between 0,3 and 0,6 dB**
- **Total Gain approximately 12/13 dB (1 stage)**
- **Noise and S-parameters Provided by manufacturer**

	Company	NF (dB)	GAIN (dB)	@Freq. (GHz)
MGF4953	Mitsubishi	0,40	13,5	12
MGF4941	Mitsubishi	0,35	13,5	12
MGF4419	Mitsubishi	0,50	12	12
ATF-36077	Agilent	0,5	12	12
MGF4931	Mitsubishi	0,60	11,5	12
NE3511S02	NEC	0,30	13,5	12
FHX13X	Fujitsu	0,45	13	12

ATF-36077 Typical Noise Parameters,
Common Source, $Z_O = 50\ \Omega$, $V_{DS} = 1.5$ V, $I_D = 10$ mA

Freq. GHz	F_{min}[1] dB	Γ_{opt} Mag.	Γ_{opt} Ang.	R_n/Z_o -
1	0.30	0.95	12	0.40
2	0.30	0.90	25	0.20
4	0.30	0.81	51	0.17
6	0.30	0.73	76	0.13
8	0.37	0.66	102	0.09
10	0.44	0.60	129	0.05
12	0.50	0.54	156	0.03
14	0.56	0.48	-174	0.02
16	0.61	0.43	-139	0.05
18	0.65	0.39	-100	0.09

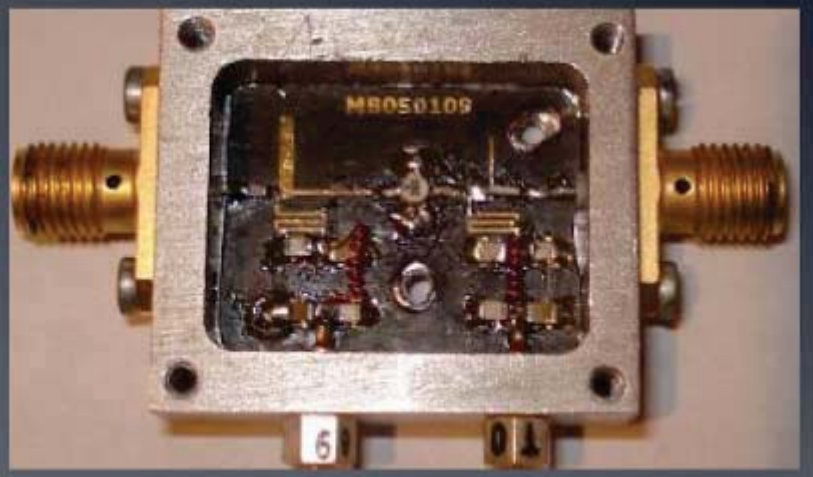
First pass: SIMULATIONS

- **S and Noise Parameters provided by the manufacturer**
- **Challenge is to create good matching networks, that will provide the lowest NF;**
- **Obtain low NF for a wide frequency band.**

Device	NF(dB @ 5GHz)	GAIN(dB @ 5GHz)
MGF4941 from Mitsubishi	0,25	13,8
MGFC4419 from Mitsubishi	0,28	12,3
MGF4931 from Mitsubishi	0,48	11
ATF-36077 from Agilent	0.38	13
NE3511S02 from NEC	0,25	13
FHX13X from Fujitsu	------	14

(Second pass: Production Example: Avago ATF-36077)

Using the Noise Parameters provided, a LNA with NF=0,38 dB and 13,4dB of gain was implemented (room T)



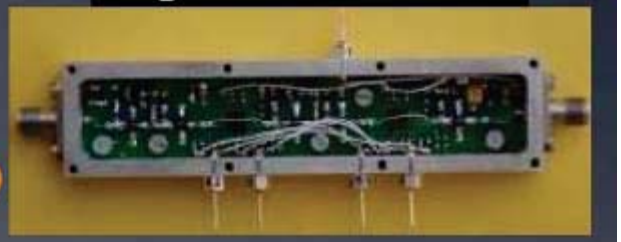
Elements for cascadable 100dB+ Gain Chain (Applied to GEM-P project)

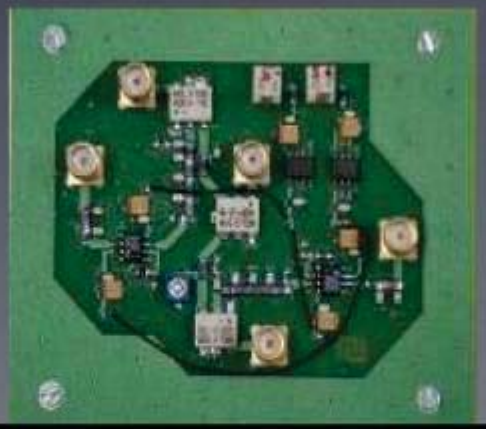
B=200MHz; 31dB; Butterworth MMIC (best response flatness)

4.9GHZ; B=600MHz Coupled Line filter RO4003

IF Chain+RF Filter

Flat gain; 71dB; Digital attenuation





120dB isolation between ports

Frequency 600MHz; VCO; MMIC Amp.; PLL synthesyzer; 7dBm

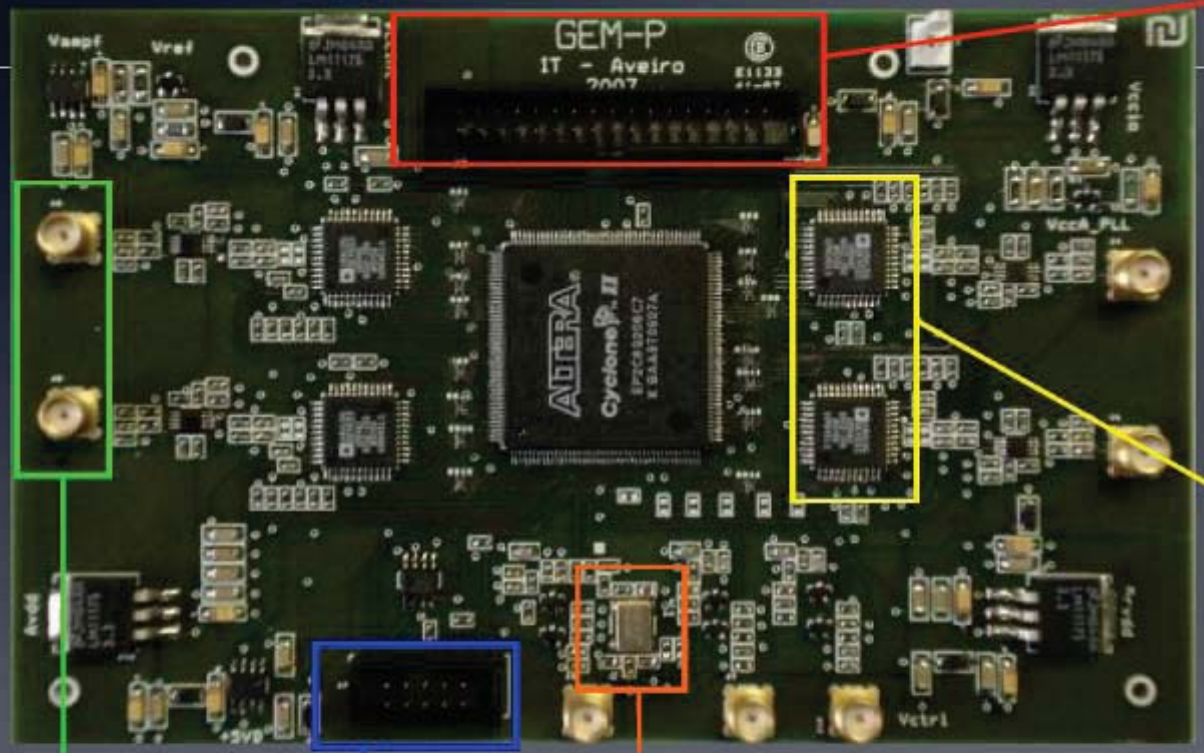
Sunpower Cryocooler evaluation

Cryotel GT model (77K nominal; operation 40K)

GEM-P frontend; InP LNAs)

(Dewar in implementation)

Digital backend (GEM)



ISA Interface output

$$RL = \Re e\left(E_{rcp}\, E_{lcp}^{*}\right) \rightarrow Stokes\ U$$

$$LR = \Re e\left(E_{rcp,-\frac{\pi}{2}}\, E_{lcp}^{*}\right) \rightarrow Stokes\ Q$$

$$RR + LL = \left\langle E_{rcp}\, E_{rcp}^{*}\right\rangle + \left\langle E_{lcp}\, E_{lcp}^{*}\right\rangle \rightarrow Stokes\ I$$

- ADCs AD9481 from Analog Devices.
- 250 Msps
- 8 bits of resolution

Analog inputs

Cristal Oscilator 100 MHz

Active Serial mode programming interface

- **FPGA** EP2C8Q208C7 **Cyclone II from ALTERA**
- 8256 LE.
- Number of 9 bits multipliers = 36;
- 208 pins
- Speedgrade 7