

CENTRAL SIGNAL PROCESSOR

AST(RON

MDA

Perentie CSP LOW CBF Update

Dr. Grant Hampson

13th November 2015 SKA Engineering Meeting perentie

CSIRO

SKA Low Correlator & Beamformer

Curtin

University of Technology



SKA Engineering Meeting 2015

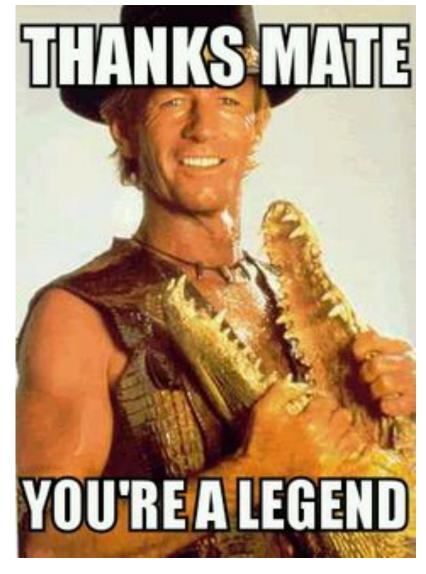
Thankyou David Loop for a great CSP presentation!

It was a tough crowd with tough questions



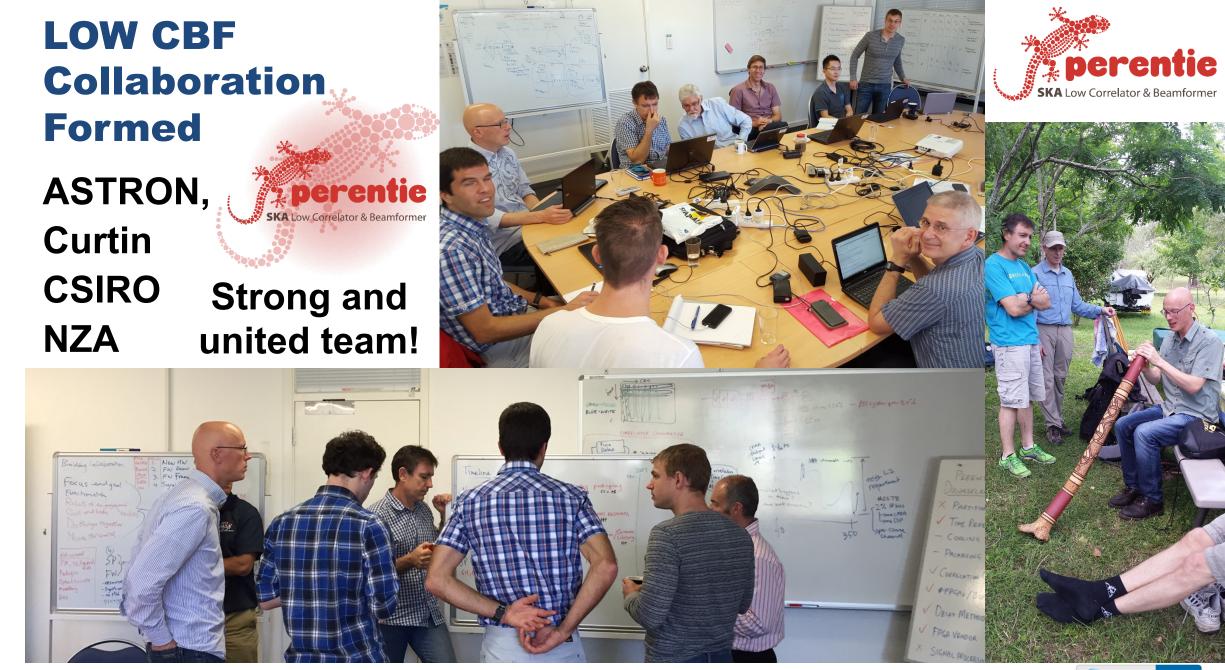
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Current LOW CBF Team

CSIRO

- Grant Hampson
- John Bunton
- Andrew Brown
- John Tuthill
- Tim Bateman
- Daniel George
- Yuqing Chen

ASTRON

- Andre Gunst
- Hajee Pepping
- Eric Kooistra
- Agnes Mika
- Koos Kegel
- Gijs Schoonderbeek

NZ

- Peter Baillie
- David Wilson

Curtin

Steve Ord







Resource Gaps

LOW CBF M&C Software

- Tango/GUI layers
 - ? TM, NRC Collaboration, CSIRO, ASTRON

CSP LOW Scientist

- Steve Ord departing
 - Some possible options being investigated

CSP LOW System Engineer

- Steve Ord departing
 - Very difficult (CSP wide resource)





Software Correlator



Curtin's involvement in LFAA and MWA means they are ideally positioned to develop a small SW correlator

- Existing in-house capability/instrument
- Sufficient for up to 4 stations, doesn't require SDP, TM, etc.



Array Release 1 (AR1) will contain 8 stations

Complete end-to-end LOW system using a FPGA correlator



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LOW CBF Approach



- The collaboration is approaching the design in a genuine, open-minded and consultative manner
- Everyone gets the opportunity to be heard

Three significant meetings:

- Jul'15: Edinburgh Planning
 - Collaboration meets for the first time, understanding approaches
- Sep'15: San Francisco Kickoff / Icebreaker
 - Engineers meet and options tabled
- Nov'15: Sydney Downselect / Delta-PDR
 - All major design decisions made foundations set
 - Commenced writing documentation for Delta-PDR submisssion for end-Jan'16



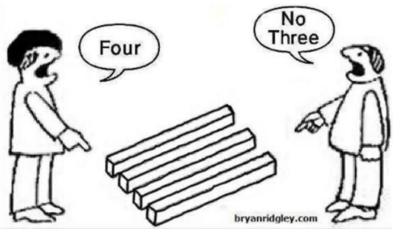






All key downselects have come to an agreeable conclusion ready for Delta-PDR:





☑ Time Reference

✓ Precision Time Protocol (PTP) distributed via Ethernet switch using existing M&C path.

Delay Method

✓ Phase shifts on narrow frequency channels shown to be optimal for LOW

Correlation Cell

✓ Hybrid ASTRON/CSIRO cell design with special input distribution circuit





Hardware Downselects

FPGA Vendor

✓ Xilinx Virtex Ultrascale+ in pre-construction period.

#FPGAs per board

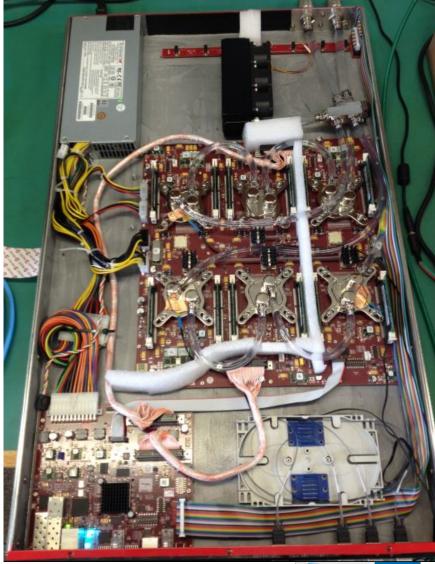
✓ one FPGA, unless firmware partitioning shows otherwise

✓ Cooling

✓ Primarily liquid for high power components as well as internal air circuit.

Packaging

✓ Pizza box as long as suitable IO and optical circuits/cabling solutions are in place







Hardest Downselect

Partitioning of FW onto HW – Filterbanks combined and separate COR/BF, later further optimisations may be possible.

Most complex downselect to resolve, effecting

- Firmware development
- Power consumption
- Testing time
- Number of cabinets
- Possible redundancy

Full optical interconnect allows change without major consequences

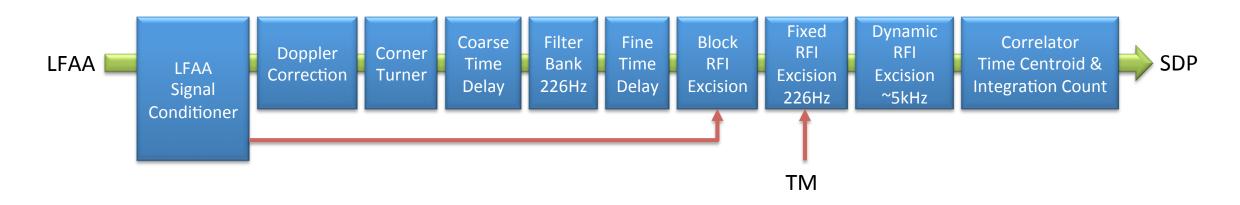






Algorithm Downselects

Signal Processing Model – RFI excision, Time Delays, Correlator Channel accumulation agreed.



With all these downselects we can commence the Delta PDR since we have agreed on this



Where to next?

LOW CBF Meetings and Workshops



- Penticton 9-13th November 2015
 - SKA Engineering Meeting + CSP meeting (now!)

- DSP Modelling Webex
 - Weekly with David Wilson to progress golden signal processing model
- Christmas 2015 Delta-PDR draft complete
- Mid-Dec / Jan SKAO Delta-PDR Progress Reviews
- End January 2016 Delta-PDR submission



LOW CBF Meetings and Workshops

- 15-19 Feb: Prototyping Workshop
 - Delta-PDR review day at ASTRON with SKAO present ?
 - Ver A Board discussion Components, software training, downselects
 - Progress on Firmware Demos & Framework
- April 2016 CSP wide TIM#5 team meeting
 - Madrid? Sydney?
 - DSP Model demonstration
- Pre-CDR Review Sep 2016
- SKA Engineering Meeting (Stellenbosch): 2nd 6th October, 2016
- Sub-element Pre-CDR Dec 2016
- SKAO: CDR Review March 2017





Delta PDR Deliverables for Low.CBF



See CIDL collection 130 on docushare (and CSP SOW)

1	Contrib	outions to:						
			SE-6a	Interface Control Document CSP to INFRA (S	SE-6a)		N. Loubser	100%
2	Contrib	outions to:	SE-7b	Interface Control Document LMC to CSP Sub	b-elements (SE-7k)	S. Vrcic	50%
			SE-7e	Interface Control Document Low Correlator	r and Beamformer	to Low PST (SE-7e)	W. van Straten	50%
2			SE-7f	Interface Control Document Low Correlator	r and Beamformer	to Low PSS (SE-7f)	B. Stappers	50%
J.	EA-1	SKA CSP SKA1-Low Array Cor	relator Sub-element	Requirement Specification (EA-1) S. C	Ord 5	0%		

Λ				
 .	EA-4a	SKA CSP SKA1-Low Array Correlator Sub-element Detailed Design Document (EA-4a)	G. Hampson	50%
5				
J .	Proto-LOW	Prototype Plan for LOW CBF	G. Hampson	50%



- 6. Risk Register (see collection 717)
- 7. Compliance statement (could be via EA-4a appendix)
- 8. ILS/RAMs spreadsheet (collection 1823, drs email Aug 14)
- 9. Pre-construction "Plan" tailoring of CSP PMP/SEMP
- **10.Costing Spreadsheet (rolled up into PM-7)**
- 11.Contributions to EICDs: LFAA, SDP, SaDT



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EICD Progress (1)



LOW.CBF-SDP

- Major sticking point use of SPEAD across multiple FPGAs is a major availability risk
 - SDP now appreciate problem
 - Solution for LOW single frequency channel per HEAP
- Every thing else in reasonable shape

LOW.CBF-SADT timing

- First discussion on this for LOW.CBF
- Agreed SADT provide necessary input for Precision Time Protocol (PTP), CSP will use PTP enabled switches

LOW.CBF-SADT-SDP

- Richard Hughes-Jones has discussion document. Reviewed and agreed
- Note SADT supply QSFP28, but not installed as front panel pluggable
- Packet address from SDP via TM







EICD Progress (2)

CBF.LOW-INAU

- All items from previous telecon now in ICD. These were checked off and agreed.
- TBC on rack load, currently 500kg, need to increase

LFAA-SADT-LOW.CBF

This will disappear, distant station via LFAA data network. Simpler ICD structure

LFAA-LOW.CBF

- Responsibility passing to ASTRON for completion
- Agreed items from previous telecom not updated in ICD
- Major sticking point LFAA have 2 stations on 40G link 256 MPO connections
 - We want fewer fibres saves 10% hardware, 2% power
 - Prefer 4-6 stations on 100G link, or 3 stations (34Gb/s) on 40G link
 - LFAA to look at possibility of 3 stations on 40G link





PDR Content

Instructions from Dave, Phillip, Marco

- To meet time and resource constraints, we have to address the logical/functional aspect rather then the physical implementation.
- I am not saying do not work on the technological aspect, of course it is important because there are several risk associated with it, but as 'preliminary' design I believe it is more important to proof the design compliancy even if the design is only functional/ logical. Hence the DDD has got the compliancy matrix section and it should be fully documented to support the system PDR.



Project Data and Tracking



Docushare

All documentation - thankyou NRC

Google docs

Prototype plan and DDD

Redmine

- Issue and task tracking
- Divided by work package

Subversion

- Coming soon will be connected to Redmine
- All FW, SW and HW source files

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Plan for the CRR LOW CR

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Perentie CSP Update 13th Nov 2015

Publications

- National Radio Science Meeting (NRSM) URSI
- Boulder 6th 9th January 2016
- "SKA LOW Correlator" special session on SKA

Conference suggested by SKAO

- SPIE 26th June 1st July, UK
- 30 May paper 6 pages
- 15th Dec 2015 submission 500 words



COMMISSION J, Radio Astronomy David DeBoer, (510) 520-9077, ddeboer@berkeley.edu TOPICS Atacama Large Millimeter Arrav – Systems and Science Digital Developments Timing and Transients SKA Technical Development Emerging Instrumentation and Techniques

- *New telescopes, techniques, and observations*
- Timely technical tutorials



2016 Prototyping Activities

New hardware

- Version A of the FPGA board
- FW Demos
- Working demonstrations of PTP, 100GbE, Optics, HMC, partial reconfiguration
- **FW Framework**
- Common library, M&C system, register file, board support package
- **Signal Processing**
- Resource estimates, some development of high risk parts





Version A Board

- April June 2016, Andrew Brown @ ASTRON
- Gijs and Andrew co-design and implementation
- Name is TBD



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Risks



List of over 100 risks have been compiled from various sources

- Many similar/duplicates
- Now have new systems engineer, categorising and rationalising the Risk Register to be updated and reviewed

Major Risks

- Manpower Resource (especially SE and Software)
- Distributed Team
- Under staffed or indecisive SKAO
- Newness of Collaboration
- Short time frame to complete delta-PDR
- Power budget exceeded
- Cost budget exceed
- Requirement churn/incompleteness (transients?)
- Inaccurate match of resources required to hardware
- New components not meeting performance/delivery goals





Perentie Monitoring and Control

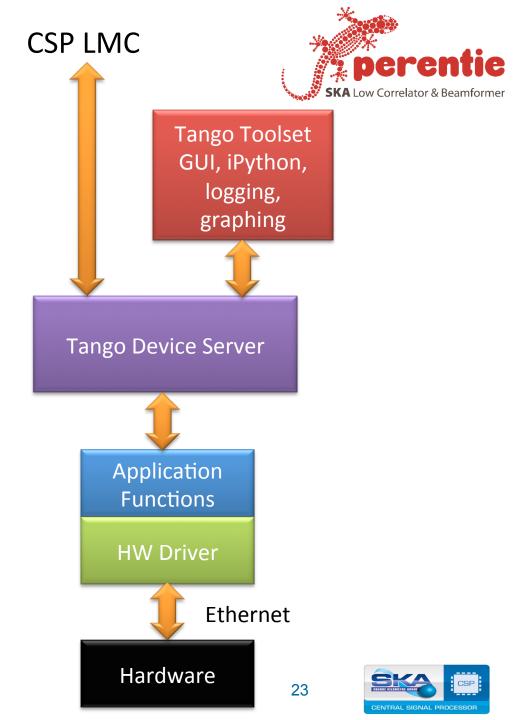
Desire for standardisation

- HW communications (AXIoE?)
- Tango software environment

LMC/TM Interface enables the telescope manager to control the system and provide operator GUIs

• GUI's not a L3 requirement ?

Work in progress to determine responsibilities (TM, LMC and CBF)



Work Status Report



- L3 Req't (highlight key assumptions)
- Pretty good shape Steve to complete before departure
- Status of DDD and compliance statement (do you meet all req'ts?)
- Transferring PIP to DDD and sections allocated to team
- External interfaces for sub-element (all relevant EICDs and IICDs) what's left to resolve? What are the remaining dependencies?
- Pretty good shape (see previous slides)
- Power estimates and refinement plan when will we know what we need to?
- Require more info from prototyping to reduce error bars
- Signal Models golden model by TIM#5
- Work in progress, tracking closely, but departure of Steve could slow progress
- Key Risk Register and TPMs walkthrough
- Review in progress, however existing TPMs require more refinement due to some design changes
- **Prototype Plan traced to risks and TPMs**
- Existing plan being reworked and new TPMs being formulated
- Stage 2 Plan including resources starting Mar 2015
- Plan in progress and most resources secured against deliverables







Questions?

Thankyou to the CSP and SKAO teams!

