

Experiences from Commissioning MWA Digital Receivers

Prabu Thiagaraj - RRI

CONTRIBUTORS

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Brian C, Miguel F M, Edward M, Andrew W
Bob Goke, Tom Booter, Randall W, MWA colleagues
Curtin, CSIRO, ANU and RRI

2019 SKA SHANGHAI MEETING 25-28 November 2019



The MWA Digital Receiver

2019
SKA
SHANGHAI
MEET



- 1 SKA-Low site in Western Australia
SKA Precursor telescope - MWA



- 2 128 Antenna Digital receivers-2012
Design / HW / FW / Commissioning

- 3 International team



M&C Meeting

Vani, Madhavi, Kamini, Vinutha, Ragavendra, Brian, Bob and Ed

Project Meetings

Receiver Digital Boards for 512T A Status Update

CONTRIBUTORS
D. Anish Rosh, Frank H Briggs, John D Burton, A.A. Deshpande,
M.R. Gopalakrishna, Grant Hampson, P.A. Kamini, Jonathan Kocz,
Dhruv Kumar, S. Madhav, Joseph Padikkumbur, T. Prabu,
Robert J. Sault, N. Udayashankar, K. S. Shivani, Mark Wilkinson
and MWA Collaboration

Digital Receiver - an update

Project Meeting Melbourne 5-8 Dec 2011

MWA
Murchison Widefield Array



- 4 Industry and academia
involvement: Design -
Assembly - Validation

- 5 Student Participation

- 6 Relevance & beyond

- 7 Agile



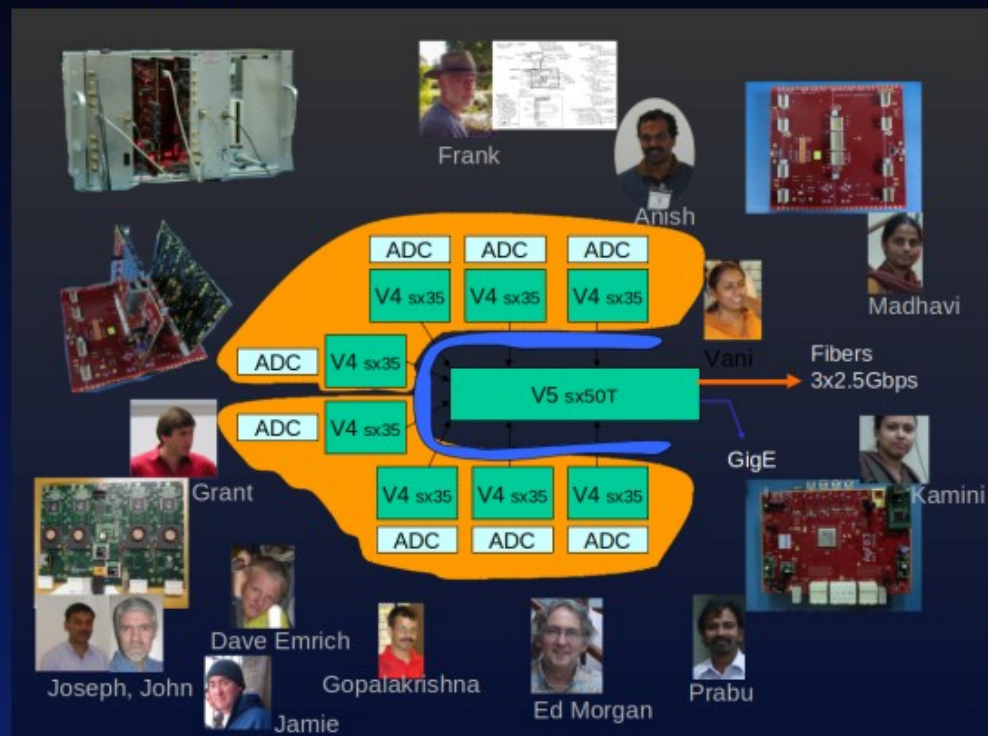
We acknowledge the Wajarri Yamatji people as the traditional owners of the Observatory site.



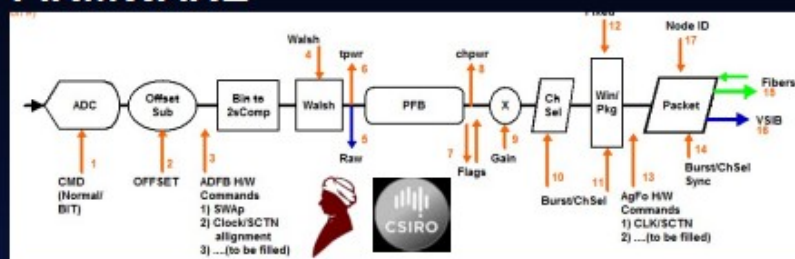
Design – PREPRODUCTION

COMMISSIONING

HARDWARE

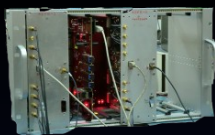


FIRMWARE



Preproduction





The MWA Digital Receiver



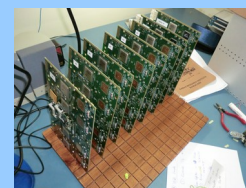
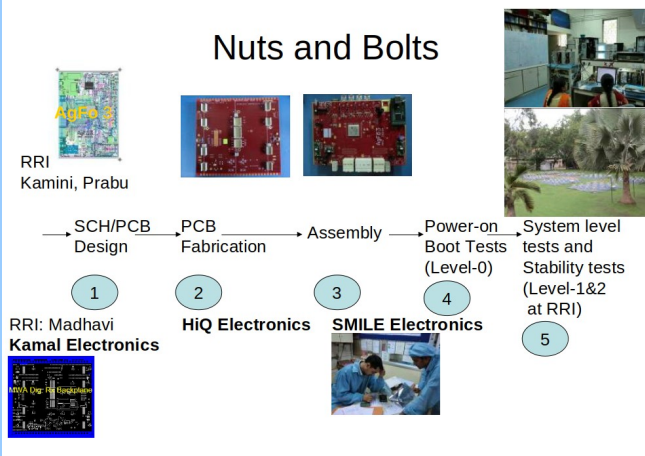
PRODUCTION

TESTS

COMMISSIONING

OPERATION

Nuts and Bolts



Receiver Cards

USB cards



AgFo card



Digital Receiver with V3 AgFo and V3 Backplane

32T mode Tests Verified

ADFB cards



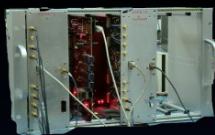
Backplanes



Digital Receiver Cards in a cage

1. Digital Receiver Cards Manufactured
2. Assembled and Tested
3. Shipped to Curtin / MRO





The MWA Digital Receiver



PRODUCTION

TESTS

COMMISSIONING

OPERATION

DESIGNED FOR TESTABILITY

Test coverage

- 1) Physical
- 2) Power
- 3) Clock
- 4) Component level: FPGA, Fiber
- 5) Integrated tests
- 6) Digital system
- 7) Functional
- 8) Alignments
- 9) Start/stop
- 10) Power Cycle
- 11) Early Mortality: 15 days
- 12) Environmental

REPEATED MANY TIMES



Firmware

Diagnostic modes

Covering:

ADC

Buffers

Channelizer

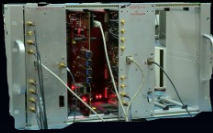
Band pass monitoring

Total Power monitoring

Fiber data

Device up & up-time tests

M&C checksum



The MWA Digital Receiver



PRODUCTION / TESTS

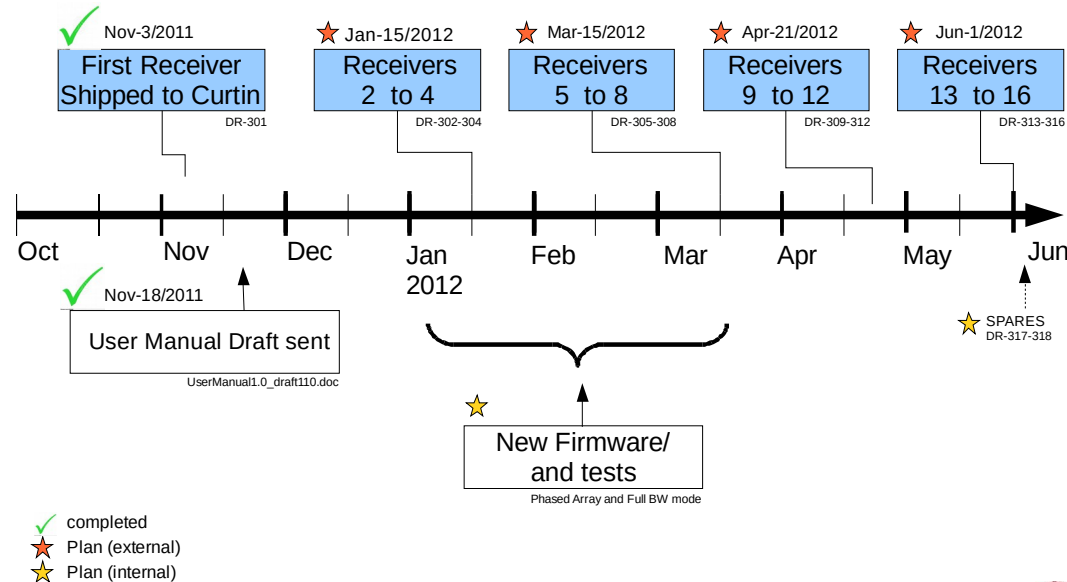
SHIPMENT

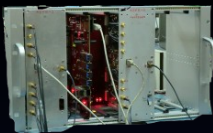
COMMISSIONING

OPERATION

Digital Receiver Delivery plan for 128-T

Shipping of receiver board sets from RRI and other plans





The MWA Digital Receiver

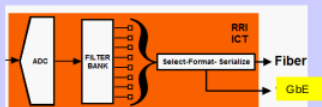


PRODUCTION

TESTS

COMMISSIONING

OPERATION



Multiple Layers



1. Internal to Digital Receiver/SBC/DAS
2. ASC and Digital Receiver
3. Beamformers, ASC and Receiver
4. Tiles, Beamformers, ASC and Receiver
5. Source Scan – autos, crosses
6. Between Receivers - crosses

Assumes:

- a) Power
- b) Clock
- c) SCTN
- d) USB → SBC
- e) GbE → Computer/Laptop

plan

128 tiles laid

Tested in sub-arrays of 32 tiles

Five sub-arrays:

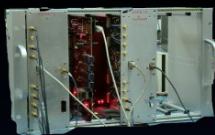
Alpha, Beta, Gamma, Delta and Epsilon

Sub arrays overlapped with tested tiles



AUG 27/12

DEC 17/12



The MWA Digital Receiver



PRODUCTION

TESTS

COMMISSIONING

OPERATION



Alpha receivers (32 tiles)
commissioned
with verification
conducted from MRO site

plan

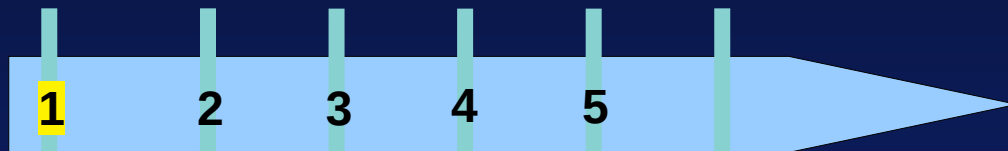
128 tiles laid

Tested in sub-arrays of 32 tiles

Five sub-arrays:

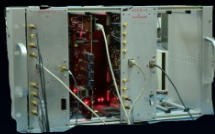
Alpha, Beta, Gamma, Delta and Epsilon

Sub arrays overlapped with tested tiles



AUG 27/12

DEC 17/12



The MWA Digital Receiver



PRODUCTION

TESTS

COMMISSIONING

OPERATION

plan

128 tiles laid

Tested in sub-arrays of 32 tiles

Five sub-arrays:

Alpha, Beta, Gamma, Delta and Epsilon

Sub arrays overlapped with tested tiles

Remaining 96 tiles
commissioned
with receivers
operated/checked
from remote

1

2

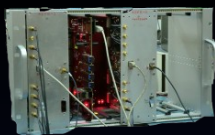
3

4

5

AUG 27/12

DEC 17/12



The MWA Digital Receiver

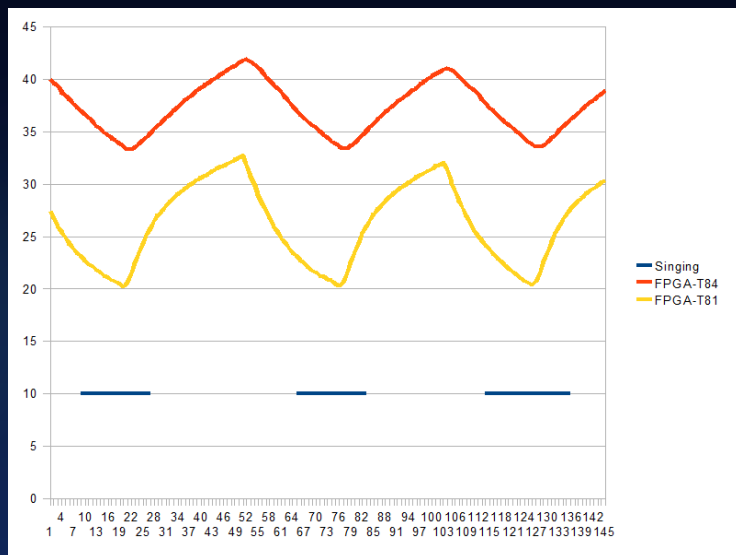


PRODUCTION

TESTS

COMMISSIONING

OPERATION



Temperature related issue

Commissioning plan

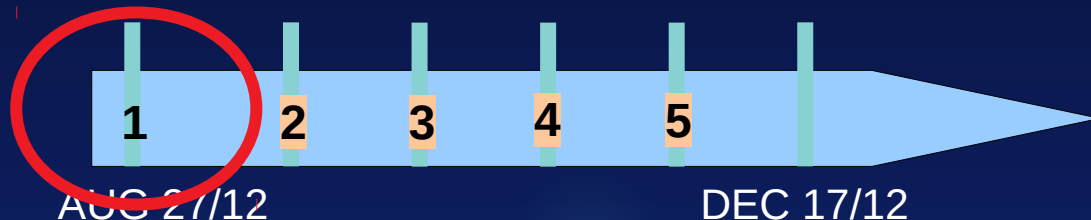
128 tiles laid

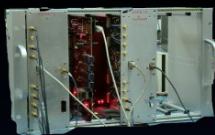
Tested in subarrays of 32 tiles.

Five sub arrays:

Alpha, Beta, Gamma, Delta and Epsilon

Each sub array overlapped with tested tiles





The MWA Digital Receiver



Lessons learned

- 1) FPGA design occupancy: **20 – 30% head room**
- 2) Clocking: **10 % head room**
- 3) Major Components: **FPGAs and ADCs**
- 4) **Spare planning:** aligned with needed up time
components 10% - digitizer 5 % - Storage
- 5) **Lightning – wind - rain**
- 6) **Test for site conditions - container inside container**
- 7) **Stress tests – temperature cycle +/- 10 -20%**
- 8) **Power cycles**
- 9) **Cold & warm start tests**
- 10) **Board level tests - clock/init**
- 11) **Integrated tests - board level**
- 12) **IO interconnect tests**
- 13) **Monitoring and Control features**
- 14) **Low latency, fast & predictable response time**

COMMISSIONING

2⁷ to 2¹⁷



A nighttime photograph of the Shanghai skyline across a body of water. The Oriental Pearl Tower is prominent on the left, and the Shanghai Tower is on the right. Other skyscrapers are illuminated with various colors like blue, red, and yellow. The lights reflect on the water's surface. The sky is dark with some clouds.

Thank You

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