Mid.CBF Technical Overview and Status Update
Mid Annual Status Update Meeting 2022

Herzberg Astronomy and Astrophysics – National Research Council Canada
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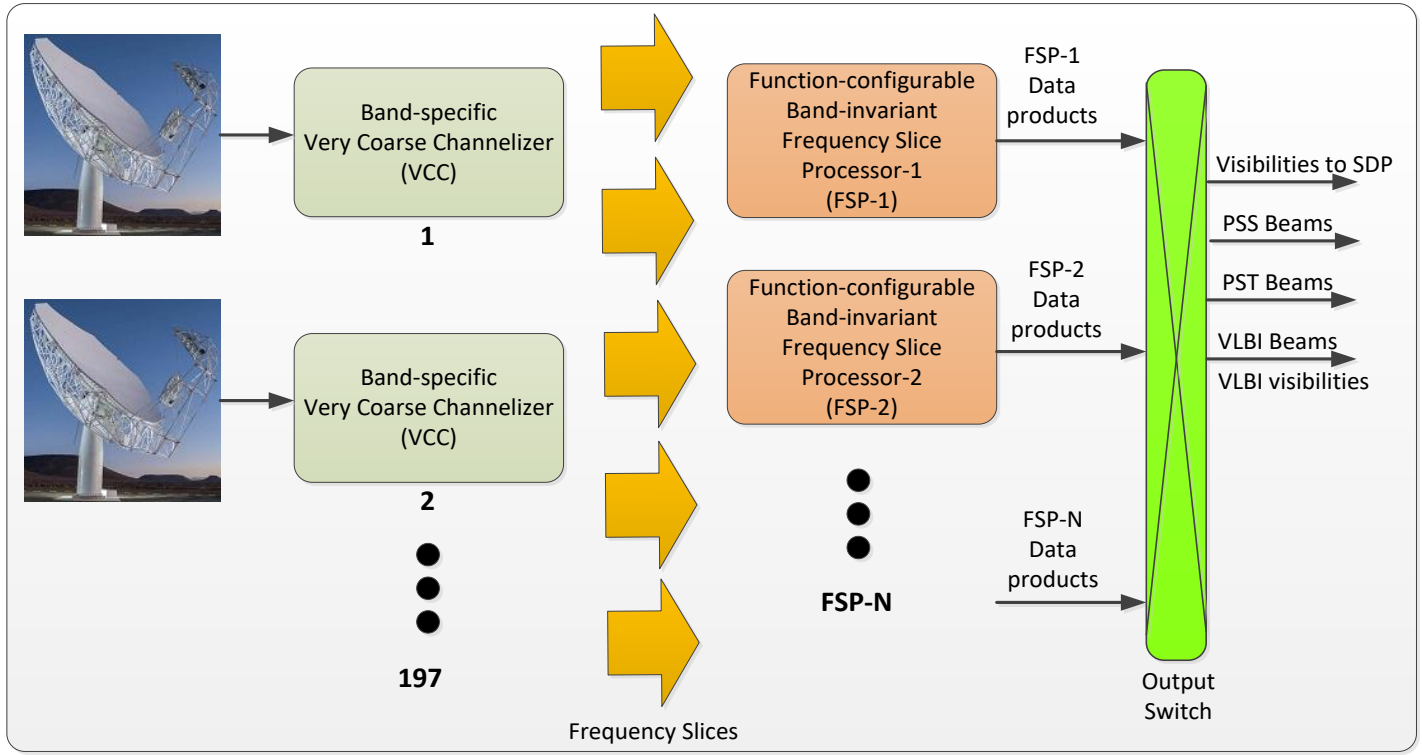
May 10, 2022

Outline

- Mid.CBF Overview in two slides!
- Updates since Mid.CBF CDR (2018)
  - Move to Cape Town + TALON Asynchronous design
  - TALON Demonstration Correlator (TDC) architecture for AA0.5/AA1
  - Hardware refresh investigation for AA2 and beyond
- Status Update
  - The Team
  - Development Progress
  - Mid PSI

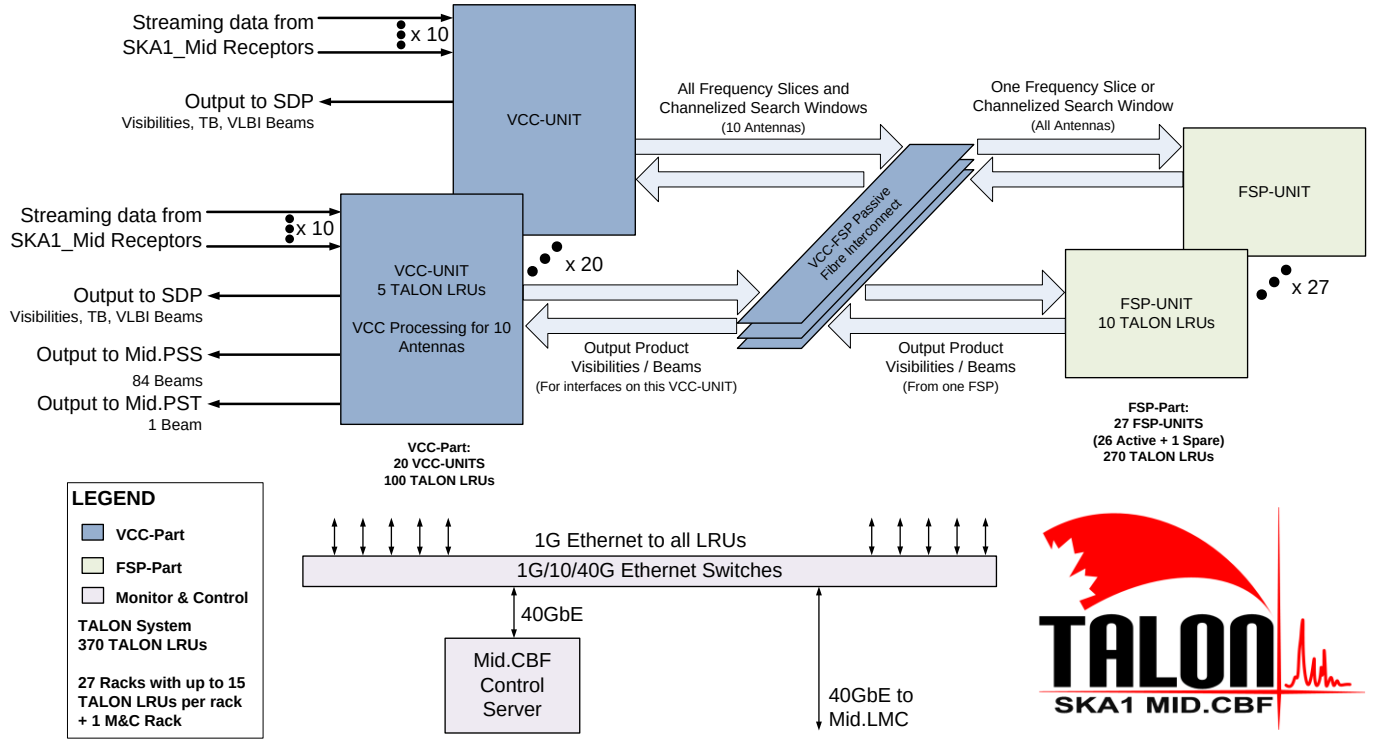
Mid.CBF Functional Overview

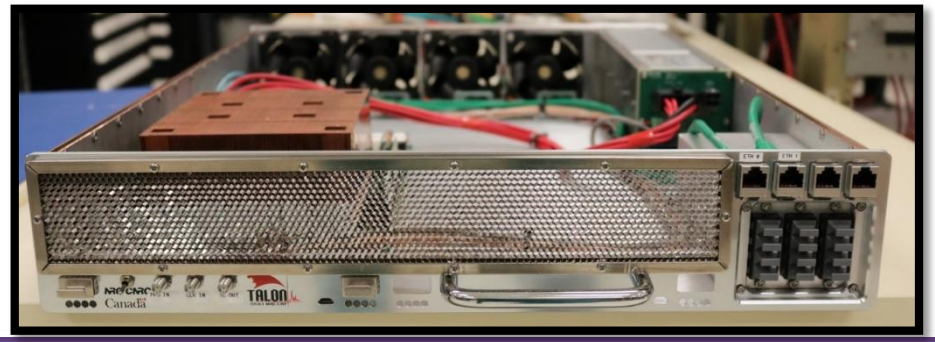
- Correlate / Beamform digitized data from 197 receptors
- Support 16 sub-arrays, with each sub-array operating in any one of the 6 SKA_Mid Bands
- Generate the following products:
  - Visibility set for up to 5 GHz of instantaneous BW
  - 1500 PSS beams @ 300 MHz
  - 16 PST beams @ up to 2.5 GHz
  - VLBI beams + visibilities for calibration
  - Zoom window visibilities
  - Transient buffer voltage data
- Processing split into two stages:
  - Band-specific Very Coarse Channelizers (VCC): one per receptor, generates ~200 MHz Frequency Slices and two 300 MHz channelized Search Windows
  - Band-invariant Frequency Slice Processors (FS): configured in one of four Function Modes (correlation, PSS, PST or VLBI) and processes one Frequency Slice or Channelized Search Window from all receptors.



Mid.CBF Physical Architecture

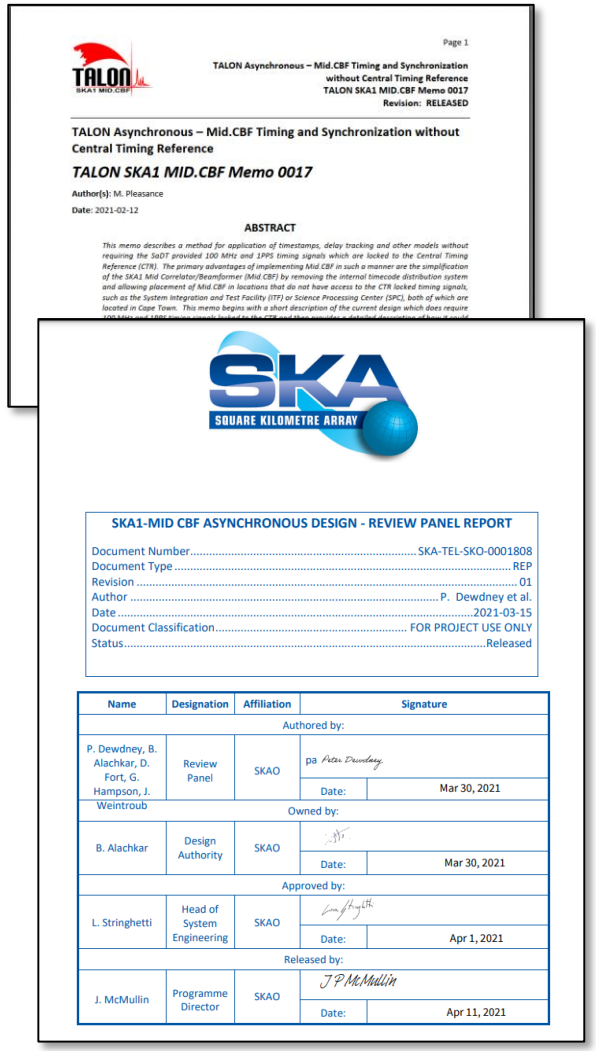
- Mid.CBF uses the custom 2U TALON LRU which houses two TALON-DX signal processing boards.
- TALON-DX has Intel Stratix 10 FPGAs, DDR4 memory + Mid-board optical modules and QSPF28 cages for IO.
- Each VCC uses one TALON-DX board and each FSP uses 20 TALON-DX FPGA boards. All connectivity between TALON-DX boards is done using point-to-point optical links which are routed via custom optical mesh LRUs.
- Mid.CBF contains 200 VCCs to support the 197 SKA_Mid receptors and 26 (+1 spare) FSPs to provide the full 5 GHz of correlated bandwidth in Band 5 and simultaneous correlation + PSS/PST beamforming in lower Bands.
- 740 TALON-DX boards
- 370 TALON LRUs
- 27 processing racks + 1 M&C rack





Move to Cape Town + TALON Asynchronous design

- ECP to move Mid PSS/PST to Science Processing Facility in Cape Town gained traction in 2020.
- Lots of benefits of moving Mid.CBF to Cape Town (AA2 and beyond) as well, but...
- Mid.CBF CDR baseline design did not “easily” move off-site
  - Baseline design used timing / synchronization scheme based on a clock and time-tick locked to the Central Timing Reference being distributed to all TALON-DX boards.
  - Aligns timing information in DSH data stream with local clock/time tick and uses local clock for processing.
  - All processing across all TALON-DX boards happening in lock-step (processing time = data time)
  - Required timing signals not available at SPF so need to do something different.
- Asynchronous TALON Design proposed in TALON Memo 17 (late 2020):
  - Uses only timestamps in the DSH data stream.
  - Performs per-receptor processing (channelization, re-sampling, delay tracking, etc.) asynchronously.
  - Delay corrected, channelized samples for a given timestamp (same data time) generated at different process times for each receptor.
  - Delay corrected, channelized samples only buffered and aligned across receptors immediately before correlation/beamforming.
  - Eliminated the need for distribution of a common clock to all FPGAs or local CTR locked timing signals
  - Reduced the amount of DDR4 required by eliminating buffering prior to delay tracking.
- Reviewed and given the nod by external panel led by Peter Dewdney in spring 2021.



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TALON Asynchronous – Mid.CBF Timing and Synchronization without Central Timing Reference
TALON SKA1 MID.CBF Memo 0017
Revision: RELEASED

TALON Asynchronous – Mid.CBF Timing and Synchronization without Central Timing Reference

TALON SKA1 MID.CBF Memo 0017

Author(s): M. Pleasance

Date: 2021-02-12

ABSTRACT

This memo describes a method for application of timestamps, delay tracking and other models without requiring the SaDT provided 100 MHz and 1PPS timing signals which are locked to the Central Timing Reference (CTR). The primary advantages of implementing Mid.CBF in such a manner are the simplification of the SKA1 Mid Correlator/Beamformer (Mid.CBF) by removing the internal timecode distribution system and allowing placement of Mid.CBF in locations that do not have access to the CTR locked timing signals, such as the System Integration and Test Facility (ITF) or Science Processing Center (SPC), both of which are located in Cape Town. This memo begins with a short description of the current design which does require

SQUARE KILOMETRE ARRAY

SKA1-MID CBF ASYNCHRONOUS DESIGN - REVIEW PANEL REPORT

Document Number	SKA-TEL-SKO-0001808
Document Type	REP
Revision	01
Author	P. Dewdney et al.
Date	2021-03-15
Document Classification	FOR PROJECT USE ONLY
Status	Released

Name	Designation	Affiliation	Signature	
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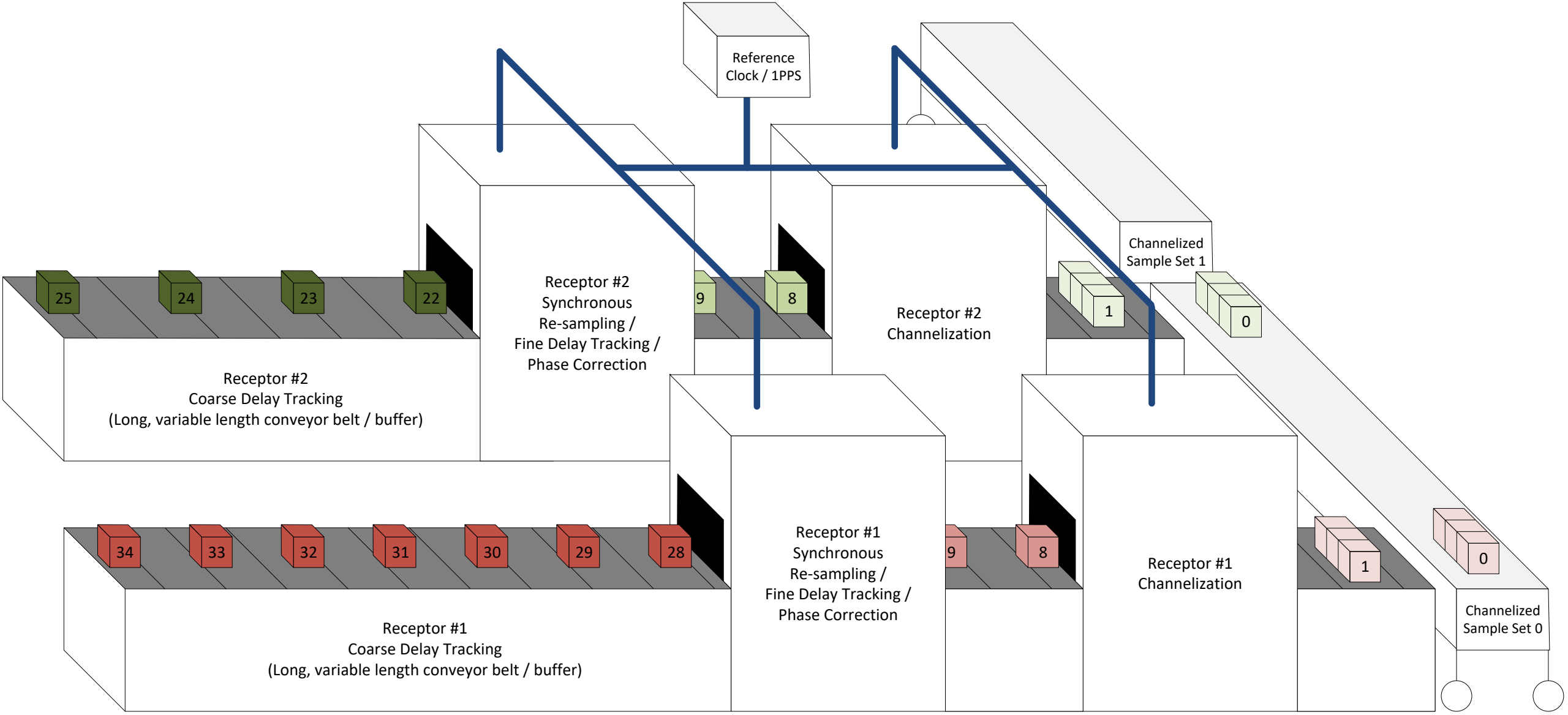
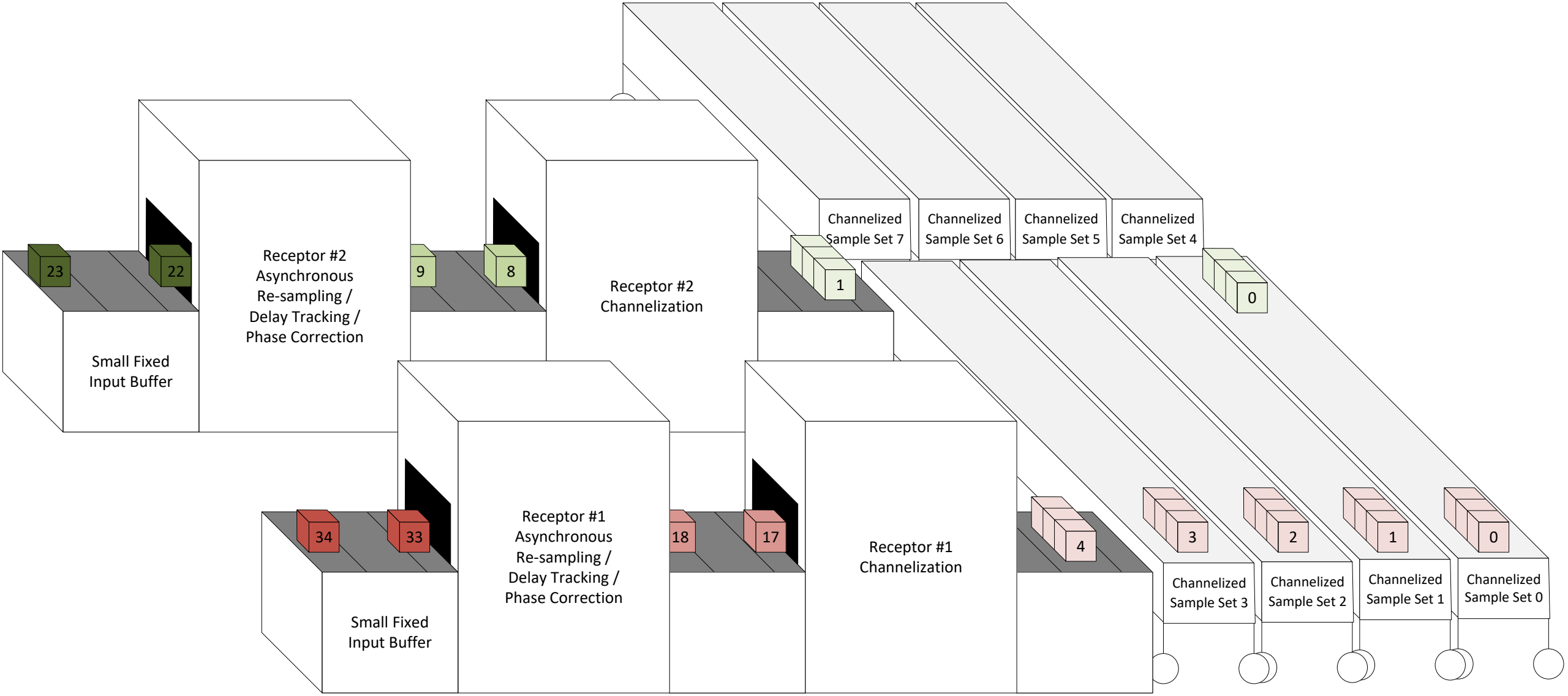
Baseline Design – Factory Analogy



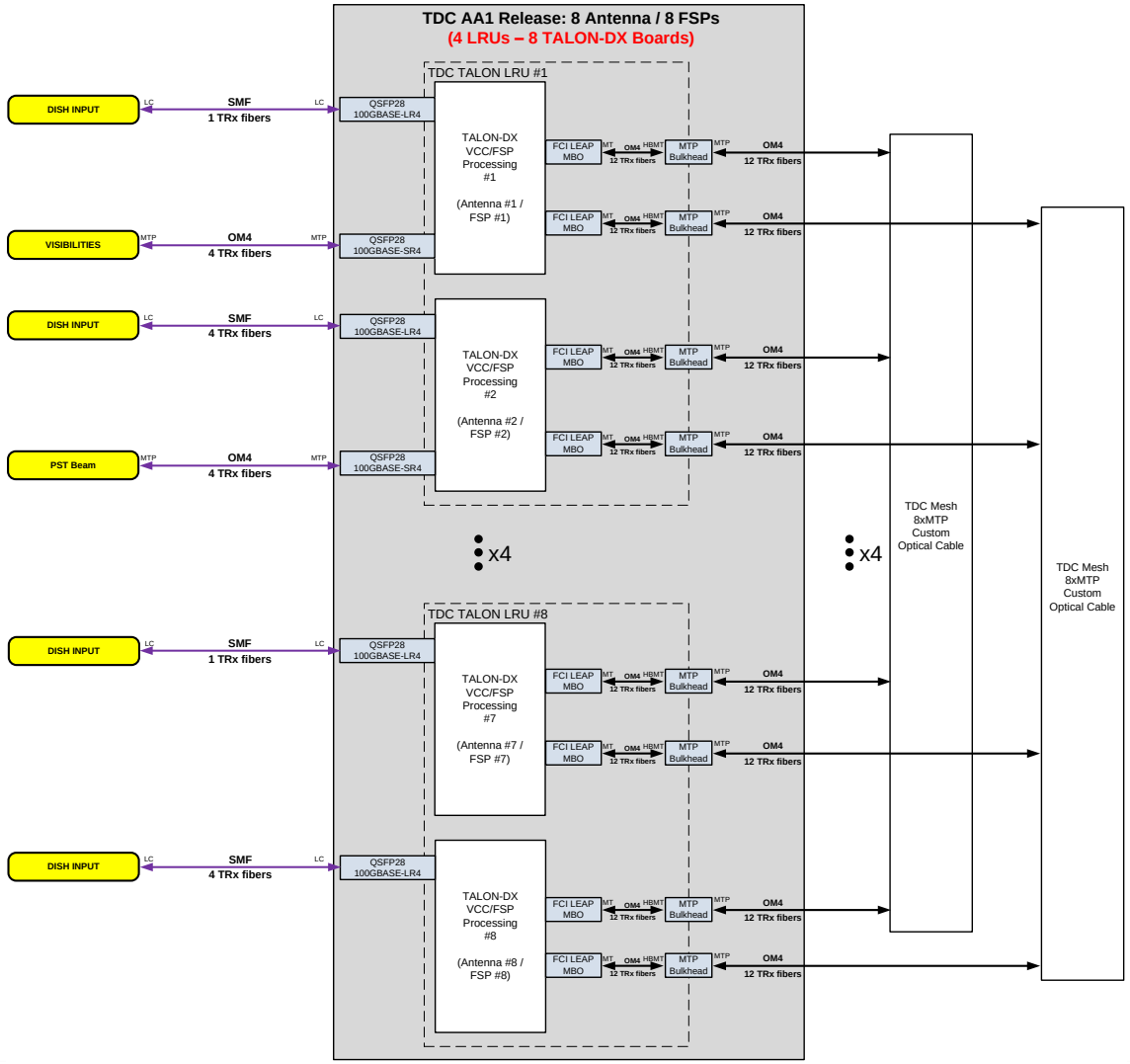
TALON Asynchronous – Factory Analogy



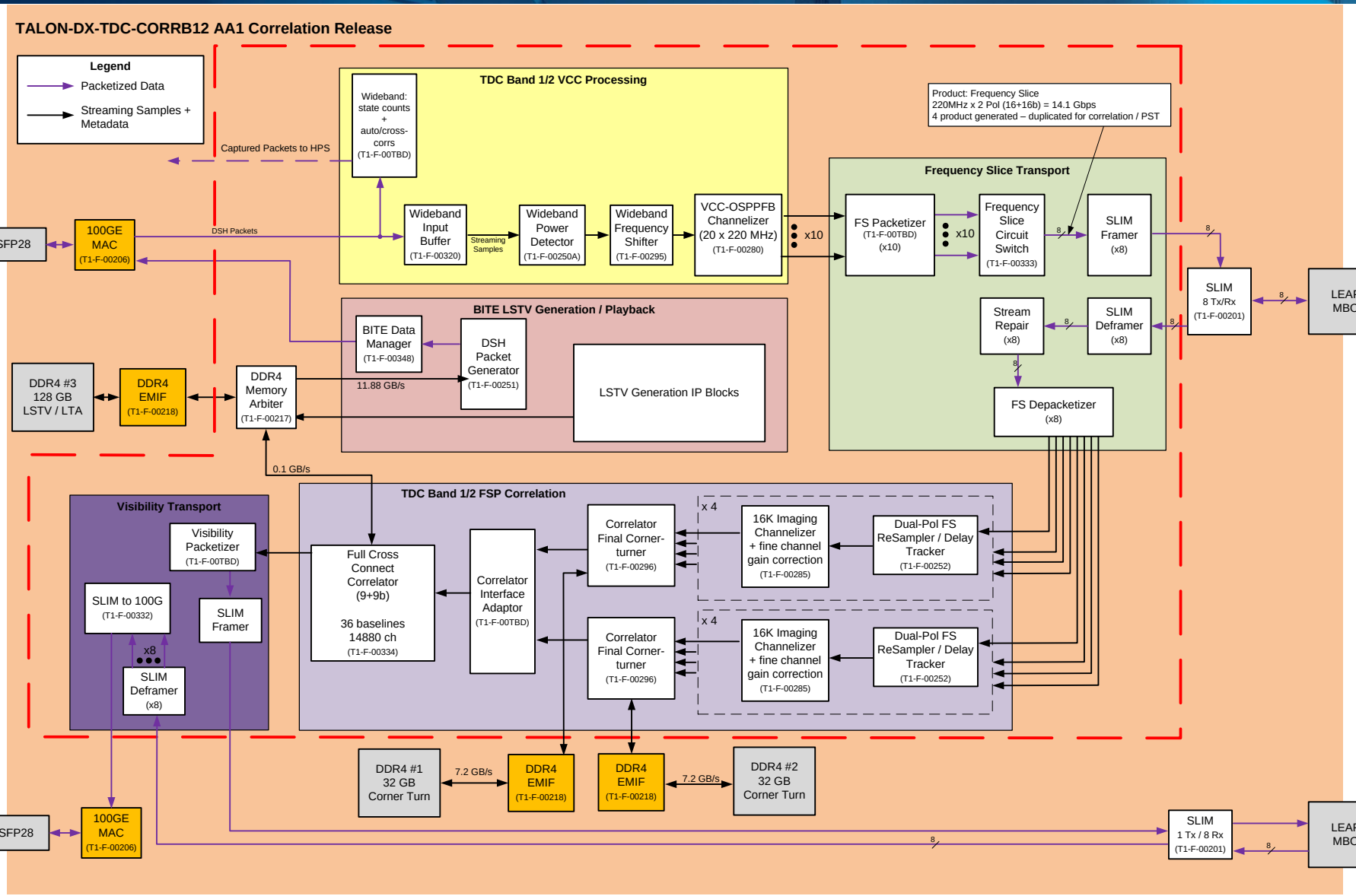
TALON Demonstration Correlator (TDC) Architecture for AA0.5/AA1

- TDC is a different physical architecture tuned for 8 receptors
- Uses identical firmware IP blocks and software to Mid.CBF wherever possible.

- Key changes compared to Mid.CBF:
  - ***WAY*** less hardware compared to using Mid.CBF VCC / FSPs
  - Signal processing done by one FPGA contains:
    - VCC processing and Frequency Slice distribution for one receptor
    - FSP processing (either correlation or PST beamforming) for a full 200 MHz FS and 8 receptors.
    - Built-in Test Environment (BITE) test vector generation
  - Much better alignment of M&C to Mid.CBF compared to earlier AA0.5/AA1 designs.

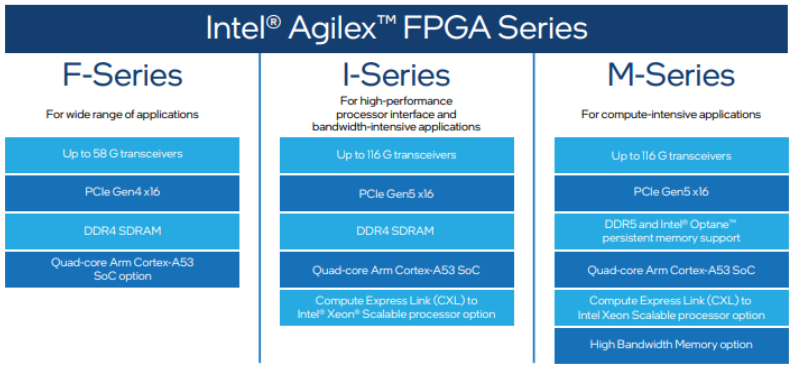


TALON Demonstration Correlator Architecture for AA0.5/AA1



Hardware refresh investigation for AA2 and beyond

- SKA construction has just begun – Intel Stratix 10 FPGA are 4+ years old.
- Next generation Agilex parts are shipping production units
- Intent has always been to investigate pros/cons of moving to newer technology for AA2 and beyond - AA0.5 and AA1 will use TALON-DX base TALON Demonstration Correlator (TDC).
- Investigating COTS products coming down the pipe – Agilex M-Series FPGA PCIe cards + 400GbE P4 Network Switch
- Hoping to leverage work done by Low.CBF
- Expect some CAPEX savings
- Expect significant power savings
- Plan to progress in PI15



45%
HIGHER PERFORMANCE*
(geometric mean versus Intel® Stratix® 10 FPGA)

UP TO 40%
LOWER POWER*
(versus Intel® Stratix® 10 FPGA)

UP TO 40
TFLOPS*

~2X FASTER
FABRIC PERFORMANCE PER WATT
(versus 7 nm competitor's FPGA)*

Status Update – The Team

- NRC + MDA team (CIPA) funded by Government of Canada through co-operation agreement between NRC and SKAO.
- Co-operation agreement runs through March 31, 2023 and is supporting the following activities:
  - Delivery of Mid.CBF for AA0.5 / AA1 – functionality for AA0.5 + hardware set for AA1
  - Support of SPFRx firmware and software
  - CSP_Mid System Engineering / I&T activities, including Mid PSI in Richmond, BC.
- Current team is around 15 FTEs and working to expand to 20+, but hiring is challenging.

- Lots of work happening to establish the in-kind contract between SKAO and NRC.
- Invitation to tender expected later in May.

Status Update – Development Progress

- Firmware:
  - TDC MVP end-to-end signal chain firmware complete and ready for testing
  - AA1 correlation firmware 95% complete – plan to start HW testing in PI15
  - Built-in Test Environment (BITE) test vector generation firmware receiving an over-haul

- Software:
  - First full vertical integration of M&C software (LMC interface -> FPGA registers) completed (PI 13)
  - Currently implementing control of VCC and FSP signal chains in Mid.CBF Control Software (MCS) and embedded Tango devices (PI 14/15/16)

- Hardware Procurement:
  - Building 16 TALON LRUs / 32 TALON-DX boards.
  - Challenging due NRC procurement process and supply chain issues.

- Critical path to AA0.5 appears to be software development and HW procurement.
- Actively working to hire and get long lead items on order.

Status Update – Mid PSI

- Mid PSI starting to take shape at MDA in Richmond, BC.
- 3 of 4 servers have been delivered and installed.
- Still waiting for delivery of last server and network switch
- Nicolas Loubser (MDA), SKA Systems Team and MDA IT all involved in getting things off the ground.
- TALON hardware for Mid PSI is available but needs to be assembled at NRC.
- Lots of exciting work coming over the next 1-2 months.

Thank you / Questions

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